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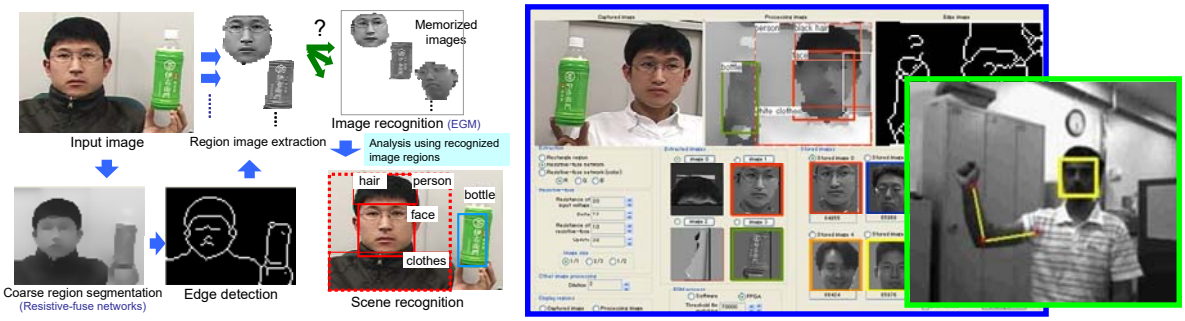
Research keywords: VLSI systems, brain-like vision systems, spiking neural networks, nonlinear dynamical VLSI systems, chaos chip, nanodevice using nanostructures on MOSFET

Major research themes, overviews, and related publications

VLSI image/scene recognition systems inspired by brain architecture

Combining some processing models inspired by brain vision functions, we have constructed a real-time image/scene recognition VLSI system that can recognize natural scenes including human faces and different objects. The processing functions used in the system are coarse region segmentation using resistive-fuse networks and image recognition of segmented regions using elastic graph matching (EGM). The scene is understood by using the relationship between segmented regions. We have also developed a face and arm gesture recognition system by combining Prof. Miyamoto's algorithm.

M. Shimizu, I. R. Khan, Y. Kuriya, H. Miyamoto and T. Morie, Markerless Arm Posture Estimation Independent of Environment, J. Signal Processing, Vol. 14, No. 6, pp. 475-481, 2010.
I. R. Khan, T. Morie, and H. Miyamoto, Face and Arm-Posture Recognition for Secure Human-Machine Interaction, IEEE Int. Conf. on Systems, Man and Cybernetics (SMC2008), pp. 411-417, 2008.
T. Nakano and T. Morie, An Image Recognition Algorithm Using Relationships between Segmented Coarse Regions, Brain-Inspired IT II, International Congress Series, pp.241-244, Elsevier , 2006.



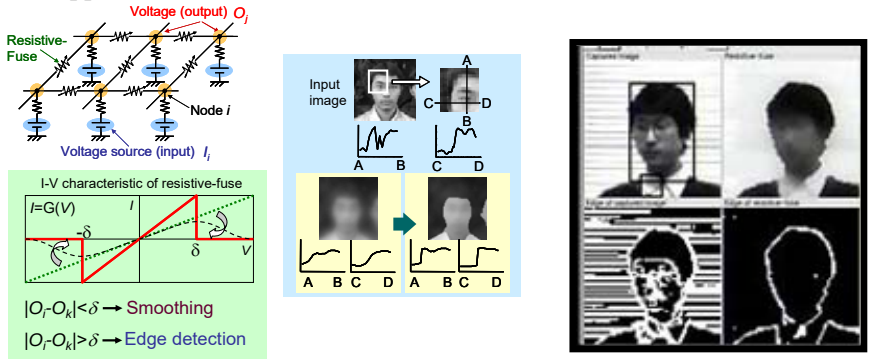
Scene recognition processing flow and outputs of real-time recognition systems.

Coupled MRF models and CMOS circuits for coarse image-region segmentation

Image region segmentation is the most important and difficult task for recognizing natural scene images including many objects. Coupled MRF (Markov random field) models are known as visual processing models that can be used for such a task. Coupled MRF models are classified into two types: region-based and boundary-based. As a boundary-based coupled MRF model, the resistive-fuse network model was originally proposed as an image segmentation method where image edges are preserved and noise is eliminated. This model can be used for coarsely segmenting images including unknown objects, because this model uses no information of the particular features of objects such as facial parts in face recognition. We have developed an FPGA-based VLSI image processing system using the resistive-fuse network model. A dedicated CMOS VLSI for resistive-fuse networks is also developed using our merged analog/digital approach. We also developed region-based coupled MRF models and CMOS circuits.

K. Matsuzaka and T. Morie, A Simplified Region-Based Coupled MRF Model for Coarse Image Region Segmentation Toward its VLSI Implementation, Proc. of Int. Symp. on Nonlinear Theory and its Applications (NOLTA2009), pp. 202-205, 2009.
Y. Kawashima, D. Atuti, K. Nakada, M. Okada and T. Morie, Coarse Image Region Segmentation Using Region- and Boundary-based Coupled MRF Models and Their PWM VLSI Implementation, Proc. Int. Joint Conf. on Neural Networks (IJCNN 2009), pp. 1559-1565, 2009.
N. Kato and T. Morie, Design of a CMOS Pixel Circuit for Coarse Region Segmentation/Extraction

Based on Merged Analog/Digital Architecture, J. Signal Processing, Vol. 11, No. 4, pp. 317-320, 2007.
T. Nakano, T. Morie, H. Ishizu, H. Ando, and A. Iwata, FPGA Implementation of Resistive-Fuse Networks for Coarse Image-Region Segmentation, Intelligent Automation and Soft Computing, Vol.12, No.3, pp.307-316 , 2006.

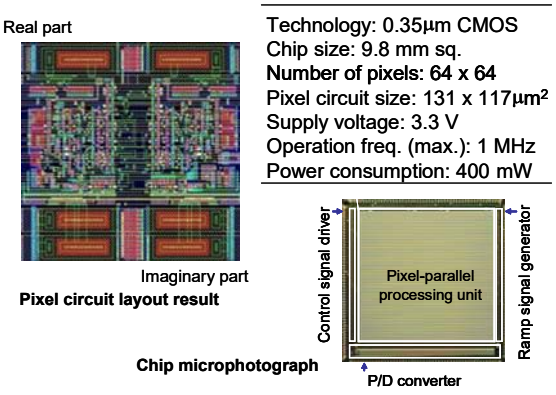


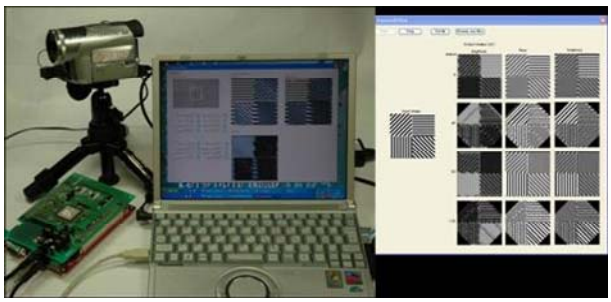
Resistive-fuse network and coarse region segmentation

Gabor-filtering VLSI chip extracting local spatial frequencies

Gabor filtering, which is a processing model of the primary visual cortex, can extract local spatial frequencies of an image. The extracted features are useful for different types of image processing such as texture analysis, face recognition. An advantage of the features is that they are hardly affected by illumination change. We have proposed a pixel-parallel algorithm for Gabor filtering using resistive networks, and a VLSI chip implementing the algorithm has been developed based on our merged analog/digital architecture.

T. Morie, J. Umezawa, and A. Iwata, Gabor-Type Filtering Using Transient States of Cellular Neural Networks, Intelligent Automation and Soft Computing, Vol. 10, No. 2, pp. 95-104, 2004.
T. Morie, J. Umezawa, and A. Iwata, A Pixel-Parallel Image Processor for Gabor Filtering Based on Merged Analog-Digital Architecture, Symposium on VLSI Circuits, pp. 212-213, 2004.





Gabor filtering system and its output

Elastic graph matching processor implemented in an FPGA for face/object recognition

The elastic graph matching (EGM) algorithm can achieve distortion-invariant image recognition. In the EGM algorithm, the same graph with plural vertices is defined on both input and memorized image planes. The pixel on each vertex is used as an evaluation point, where the pixel feature values (Gabor features) in the input and memorized images are compared. The graph of either input image or memorized one is distorted to find the better matching points. We have proposed a digital VLSI architecture for EGM, and its FPGA implementation has been developed based on the proposed architecture. This FPGA implementation is included in our VLSI image/scene recognition system.

T. Nakano and T. Morie, A Digital LSI Architecture of Elastic Graph Matching and Its FPGA Implementation, Proc. Int. Joint Conference on Neural Networks (IJCNN05), pp. 689-694, 2005.

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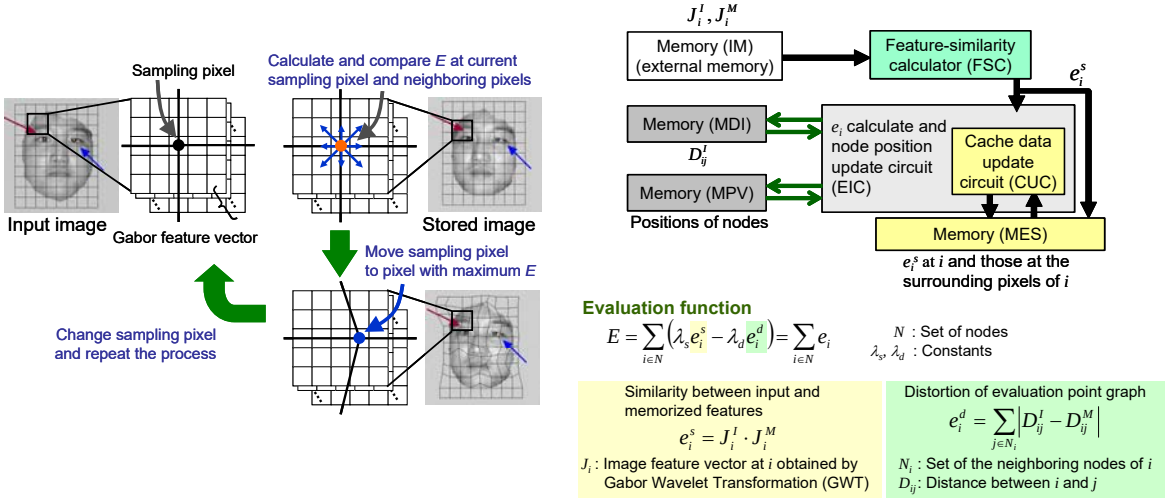
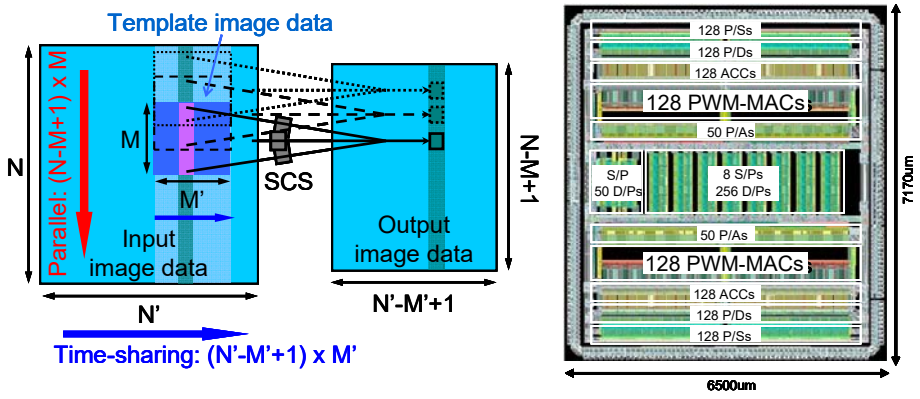


2D image matching processor VLSI based on merged analog/digital architecture

2D cross-correlation and convolution are fundamental calculations for image matching or intelligent image recognition. Both calculations are different, but can be achieved by the same VLSI architecture. It is useful for robot vision to develop high-speed, compact and low-power VLSIs for implementing cross-correlation calculations. We have developed a 2D image matching processor VLSI based on our merged analog/digital architecture. The VLSI chip has been designed using a TSMC 0.25 micron CMOS process, and it performs 6-bit-precision 2D cross-correlation or convolution operation for an input image of 256x256 pixels and a template image of 50x50 pixels within 10 msec. Its operation performance is 25.8 GOPS, and the estimated power consumption is 270 mW. We also proposed a new architecture based on a sorted projection-field model.

M. Sakai, T. Morie, M. Mitarai, and K. Korekado, Design of an 2D Image Matching Processor LSI Based on Merged Analog/Digital Architecture, RISP 2007 Int. Workshop on Nonlinear Circuits and Signal Processing (NCSP'07), pp. 81-84, 2007.
O. Nomura, T. Morie, K. Korekado, T. Nakano, M. Matsugu, and A. Iwata, An Image-Filtering LSI Processor Architecture for Face/Object Recognition Using a Sorted Projection-Field Model based on a Merged/Mixed Analog-Digital Architecture, IEICE Trans. Electron., Vol. E89-C, No. 6, pp.781-791, 2006.

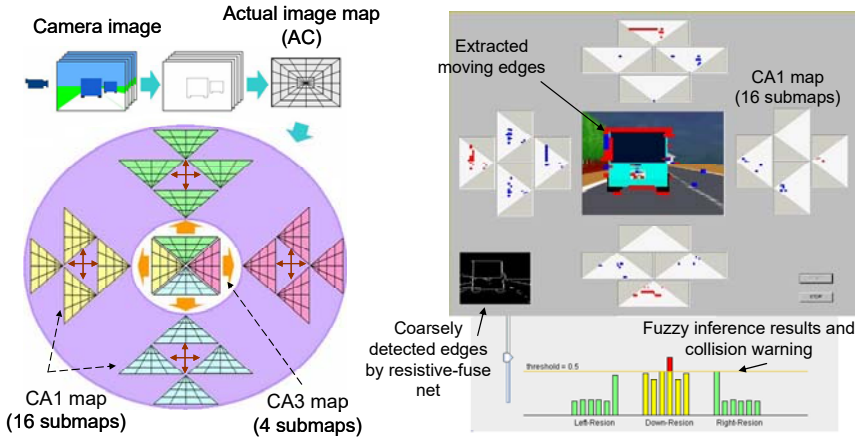


Moving-object detection model with monocular camera and its FPGA implementation for collision warning

We have developed an FPGA-based moving-object detection and collision warning system for advanced automobile driver assistance systems or autonomous moving robots. The system consists of three function blocks: coarse edge detection using a resistive-fuse network, moving-object detection inspired by neuronal propagation in the hippocampus, and danger evaluation and collision warning using fuzzy

inference. The first two functions are implemented in FPGAs. The system can detect moving objects with a speed range of 3-192 km/h with a sampling period of 30 ms for an input image of 320x256 pixels, and can output a warning against dangerous regions in the input image.

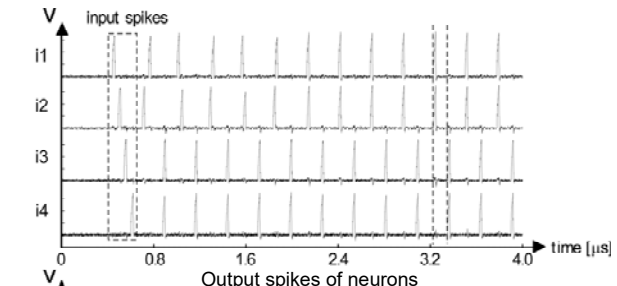
H. Liang, T. Morie, Y. Suzuki, K. Nakada, T. Miki, and H. Hayashi, An FPGA-based Collision Warning System Using Hybrid Approach, 7th Int. Conf. on Hybrid Intelligent Systems (HIS07), PP. 30-35, 2007.

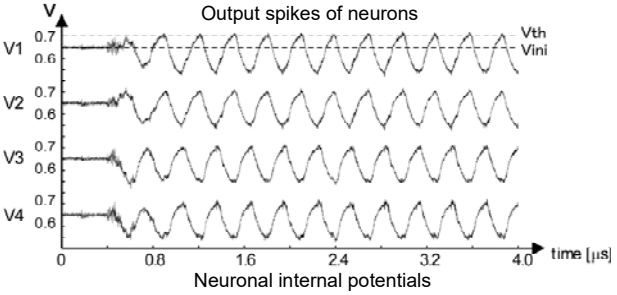


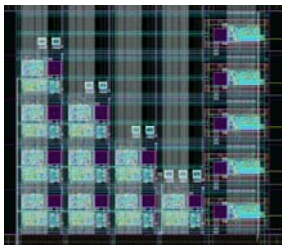
Information processing of spiking neural networks and its VLSI implementation

Spiking neuron models, which express analog information by the timing of neuronal spike firing, attract a lot of attention with expectation of their higher information processing ability. We have developed CMOS VLSI integrate-and-fire-type spiking neural networks. On the other hand, it is known that a biological neuron changes its synaptic weights by STDP (Spike-Timing Dependent synaptic Plasticity). STDP is a learning rule depending on relative timing between asynchronous spikes. There are two types of STDP which are characterized by asymmetric and symmetric time windows. We have designed both types of STDP synapse circuits, and successfully observed correct operation in VLSI Hopfield-type feedback neural networks.

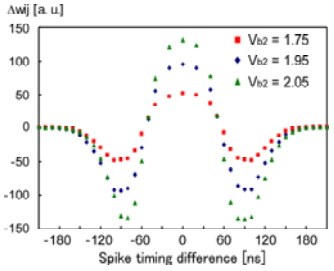
H. Tanaka, T. Morie, and K. Aihara, A CMOS Spiking Neural Network Circuit with Symmetric/ Asymmetric STDP Function, IEICE Trans. Fundamentals, Vol. E92-A, No. 7, pp. 1690-1698, 2009.
K. Sasaki, T. Morie, and A. Iwata, A VLSI Spiking Feedback Neural Network with Negative Thresholding and Its Application to Associative Memory, IEICE Trans. Electron., Vol. E89-C, No. 11, pp. 1637-1644, 2006.







Spiking neural network LSI layout result



STDP circuit measurement result

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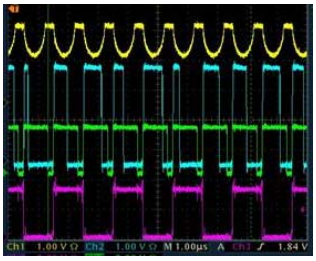
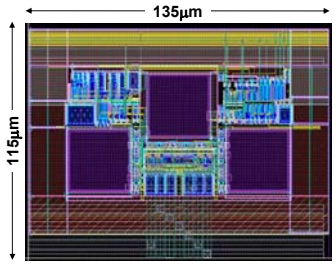
CMOS circuits for nonlinear dynamical systems (chaos circuits, phase oscillator circuits, etc.)

We have designed, fabricated, and tested arbitrary chaos generator circuits with voltage and current sampling schemes with pulse phase modulation signals. These circuits generate an arbitrary nonlinear function corresponding to the time-domain voltage or current waveforms supplied from an external source. We have also proposed related circuits for self regulatory threshold dynamics and for phase oscillators. In the latter circuit, the phase variables are represented by pulse-width modulation signals. We have designed, fabricated and tested a coupled phase oscillator circuit using a 0.25 micron CMOS process.

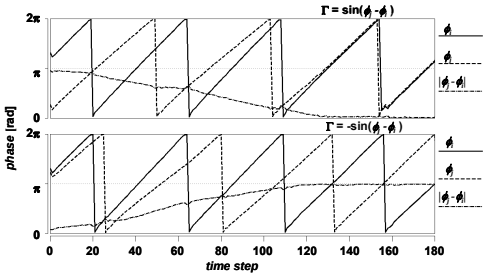
D. Atuti, T. Morie, and K. Aihara, A Current-Sampling-Mode CMOS Arbitrary Chaos Generator Circuit Using Pulse Modulation Approach, IEICE Trans. Fundamentals, Vol. E92-A, No. 5, pp. 1308-1315, 2009.
D. Atuti, K. Nakada, and T. Morie, CMOS Pulse-Modulation Circuit Implementation of Phase-Locked Loop Neural Networks, IEEE Int. Symp. on Circuits and Systems (ISCAS2008), pp. 2174-2177, 2008.
D. Atuti, N. Kato, K. Nakada, and T. Morie, CMOS Circuit Implementation of a Coupled Phase Oscillator System Using Pulse Modulation Approach, European Conf. on Circuit Theory and Design (ECCTD 2007), pp. 827-830, 2007.
D. Atuti, T. Morie, and K. Aihara, A Pulse-Modulation Circuit for Nonlinear Systems with Self Regulatory Threshold Dynamics, IEEE Int. Workshop on Nonlinear Dynamics of Electronic Systems (NDES 2007), pp. 145-148, 2007.
T. Morie, K Murakoshi, M Nagata, and A. Iwata, Pulse Modulation Techniques for Nonlinear Dynamical Systems and a CMOS Chaos Circuit with Arbitrary 1-D Maps, IEICE Trans. Electron., Vol. E87-C, No. 11, pp. 1856-1862, 2004.



Measurement result of chaos generator circuit (blue waves indicate chaotic PWM signals)



Layout result of CMOS circuit for self regulatory threshold dynamics



Measurement results of CMOS coupled phase oscillator circuits (synchorized with in-phase and anti-phase)

Pixel-parallel directional state-propagation algorithm for subjective contour generation and its VLSI implementation

An image processor LSI chip that performs directional pixel-state propagation processing has been developed using a PWM-based pixel-parallel architecture. This processing can be used for subjective contour generation, which is a typical function of the visual system in the human brain to complete the lacked natural-image information. The LSI chip has been designed and fabricated using a 0.25 micron mixed-signal CMOS process. The number of processing units included in the chip is 35x35. We have verified the propagation process by measuring the fabricated chip, and have successfully generated subjective contours of Kanizsa figures using the chip.

T. Morie and Y. Kim, A Subjective-Contour Generation LSI System with Expandable Pixel-Parallel Architecture for Vision Systems, IEEE Int. Solid-State Circuits Conf. (ISSCC2009), Digest of Technical Papers, #28.6, pp. 478-479, 2009.
Y. Kim and T. Morie, A Pixel Circuit Implementing an Anisotropic Diffusion Algorithm for Subjective Contour Generation Using Merged Analog-Digital circuit Approach, J. Signal Processing, Vol. 10, No. 4, pp. 259-262, July, 2006.

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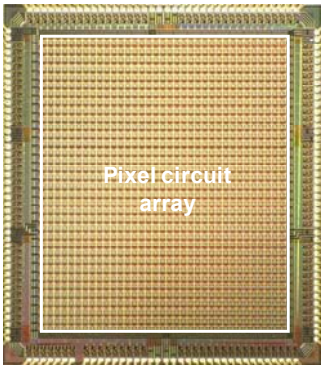
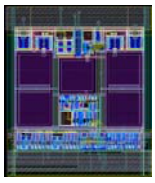


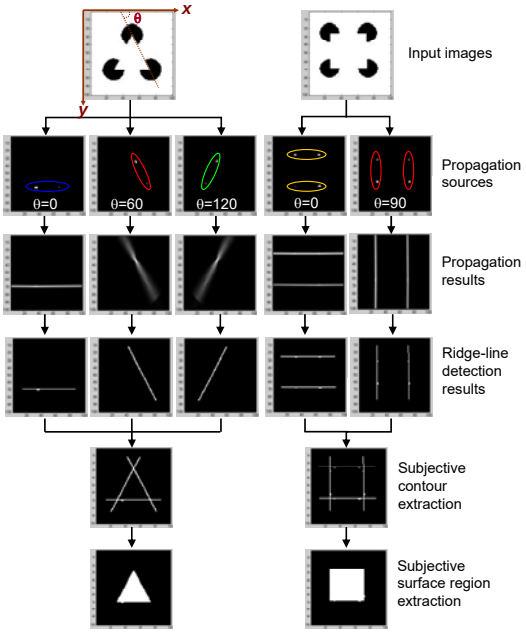
Chip microphotograph

Technology: 0.25μm CMOS
Chip size: 5.27x4.63 mm²
Number of pixels: 35 x 35
Pixel circuit size: 123x104μm²
Supply voltage: 3.3 V
Update cycle (typ.): 2.2 μs
Power consumption: 360 mW



Pixel circuit

Pixel-parallel directional state-propagation LSI

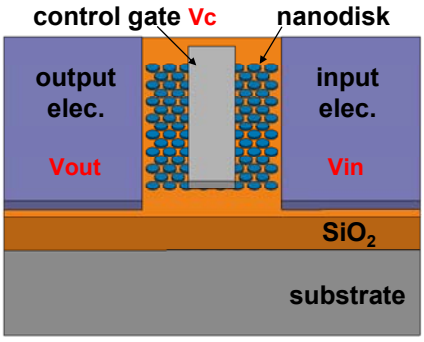


Processing flow for subjective contour generation

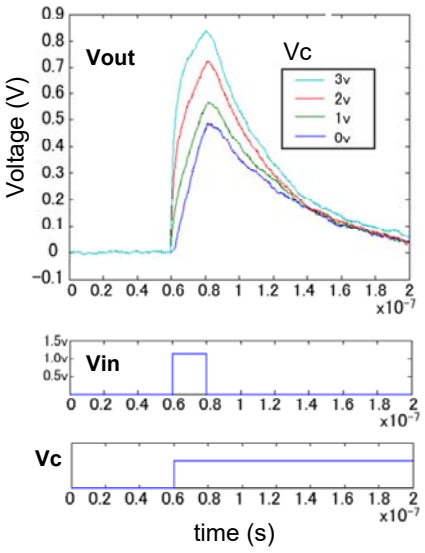
Nanostructures and CMOS circuits for Brain-like information processing

In spiking neuron models, which simplify the biological neuron, generation of post-synaptic potentials (PSPs) is an essential function. We propose a new nanodevice structure using a nanodisk array connected to a MOSFET for these models. The structure generates PSPs by taking advantage of the delay in electron hopping movement among nanodisks. The results of single-electron circuit simulation demonstrate the controllability of PSP shapes by a control gate placed over the nanodisk array.

M. Igarashi, C.-H. Huang, T. Morie, and S. Samukawa, Control of Electron Transport in Two-Dimensional Array of Si Nanodisks for Spiking Neuron Device, Appl. Phys. Express, 3, 085202, 2010.
T. Morie, Y. Sun, H. Liang, M. Igarashi, C. Huang, and S. Samukawa, A 2-Dimensional Si Nanodisk Array Structure for Spiking Neuron Models, IEEE Int. Symp. on Circuits and Systems (ISCAS 2010), pp. 781-784, 2010.



Simulation structure



Simulation results

Potential joint research topics:

We consider our different vision chips, brain-like function chips and systems as candidates for robot brains.