A multi-nanodot floating-gate MOSFET circuit for spiking neuron models

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1. Introduction

Mimicking brain functions and structures is a very important and challenging approach to perform highly intelligent information processing. In the brain, a neuron receives many electric impulses via synapses, and outputs spike pulses. Processing based on spike pulses is essential in neuronal networks. However, most attempts for hardware implementation of artificial neural networks until several years ago were based on *rate coding* models, which define analog neuronal activity as an average of pulse events over a certain time span.

Instead of such classical analog-type neuron models, recent neuroscientists are attracted to a more realistic neuron models that directly treat spike pulses, which is called *spiking neuron* models. One of the basic spiking neuron models is an *integrate-and-fire (IF) neuron model* as shown in Fig. 1. A spike pulse inputted to a neuron via a synapse generates a post-synaptic potential (PSP), which temporarily increases or decreases according as the synaptic connection is excitatory or inhibitory (positive or negative synaptic weights). The neuron's internal potential $I(t)$ is determined by the spatio-temporal summation of all PSP's. If $I(t)$ exceeds a certain threshold, the neuron emits a spike pulse.

The property of a spiking neural network consisting of IF neurons depends on the relation between average of inter-spike-intervals and the PSP decay time constant. By using various PSP decay constants, spiking neural networks should perform intelligent information processing.

A MOS device mimicking a neuron has already been proposed, which is called *neuron-MOS*, and has capacitive-coupled multiple input gates with a floating-gate [1]. This device can be used for analog-valued neuron models based on rate coding, but it cannot provide PSP characteristics because the output immediately follows the input pulses.

A neuron circuit with arbitrary PSP profiles can be realized in the ordinary CMOS, but requires many circuit components and therefore consume large chip area and power.

In this paper, we propose a multi-nanodot floating-gate MOS device for IF neurons, which achieves ultimately low power dissipation and large packing density.

2. Multi-nanodot floating-gate MOS device for IF neurons

We have already proposed the similar structure and circuit for associative memory [2, 3]. We slightly modify its structure and achieve continuous-time operation, which is essential to IF neurons.

The proposed structure is shown in Fig. 2. Nanodot array structures are constructed on a MOS transistor gate electrode. Each nanodot array structure consists of one-dimensional (1D) dot array: A_h $(D_1, \cdots, D_n, D_c, D_n, \cdots, D_1)$, where n is the number of dots at a side of A_h (in Fig. 2, $n = 5$). The center dot D_c is capacitively coupled with the MOS gate via nanodot D_v. The capacitance C_o corresponds to the gate capacitance of the MOS transistor.

Spike pulses are inputted at node IN's. An electron e_M is introduced at the center dot D_c. By applying appropriate bias voltages, the profile of the total energy as a function of the position of e_M along 1D array A_h has two peaks as shown in Fig. 3 because of the charging energy of e_M itself. The minimal values of the energy is located at D_c and both of D_1's. The energy differences can be larger than the thermal energy at room temperature even if the tunneling junction capacitance C_j is not so small.

At the stationary state without input pulses, electron e_M almost always stays at the center dot D_c although the position of e_M fluctuates by thermal noise. When a spike pulse inputs, if the pulse width is long enough and the pulse voltage is high enough, e_M quickly moves to D_1, and after the pulse ceases, e_M slowly moves back to D_c because the energy difference between at D_c and at D_1 is small.

The position of e_M affects the gate voltage V_o; i.e., when e_M stays at center dot D_c, V_o is reduced because of capacitive coupling. Because the above process occurs stochastically, V_o fluctuates due to fluctuation of the position of e_M. However, if the same input pulse is applied to a number of arrays, analog PSP is realized as the average gate voltage. PSP's generated by plural nanodot arrays are summed on gate capacitance of the MOSFET.

3. Single-electron circuit simulation results

We analyzed the proposed circuit shown in Fig. 2 by using a Monte Carlo single-electron simulator [4].

Fig. 4 shows the transition probability of e_M between D_c and D_1 as a function of time according as the input voltage changes. The shape of PSP (V_o) is approximately proportional to this probability. The time constant of PSP can be controlled by the baseline voltage of the input. Fig. 5 shows the time dependence of V_o when a pulse is inputted to one and two nanodot array(s) (one and two input cases). Voltage V_o fluctuates due to the fluctuation of electron position, but the average voltage roughly represent a PSP. The summation of two inputs can also be realized.

4. Conclusion

We proposed a nanostructure for realizing IF neurons. It can operate at room temperature. Stochastic operation of electron tunneling assisted by thermal noise generates the duration of post-synaptic potential after a spike pulse ceases. This is a unique property of this structure.

References

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[3] T. Morie, et al., *International Workshop on Quantum Functional Devices (QFD2000)*, pp. 210-213, Kanazawa, Japan (2000)

[4] T. Yamanaka, et al., *Nanotechnology*, **11**, 154–160 (2000)

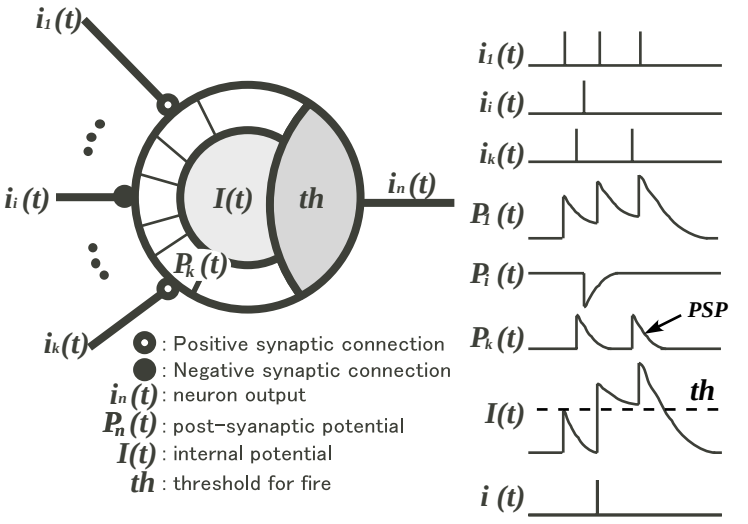

Fig. 1: Schematic of Integrate-and-Fire (IF) neuron model.

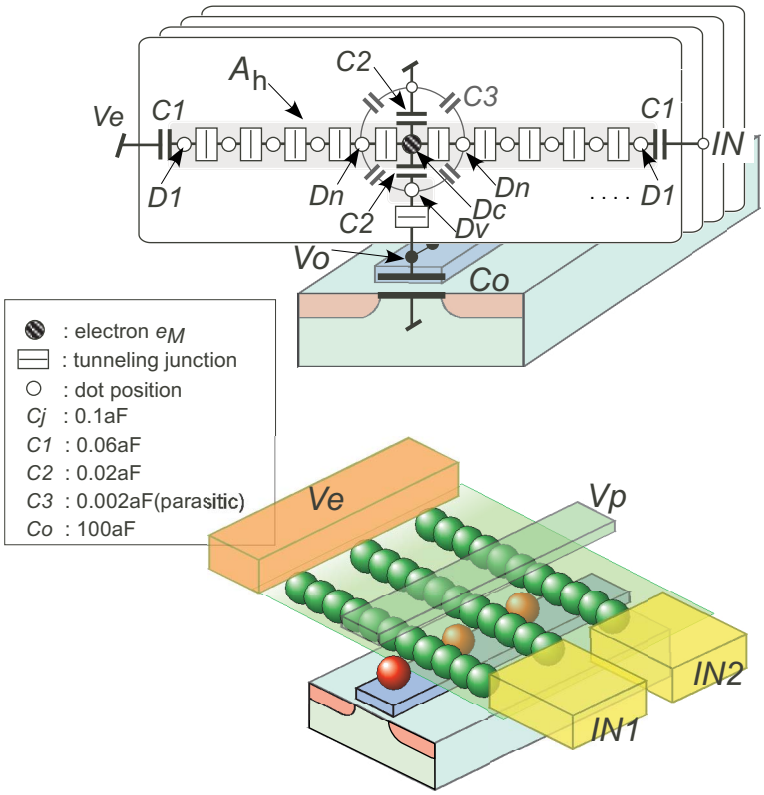

Fig. 2: Single-electron circuit and nanostructure for IF neuron model.

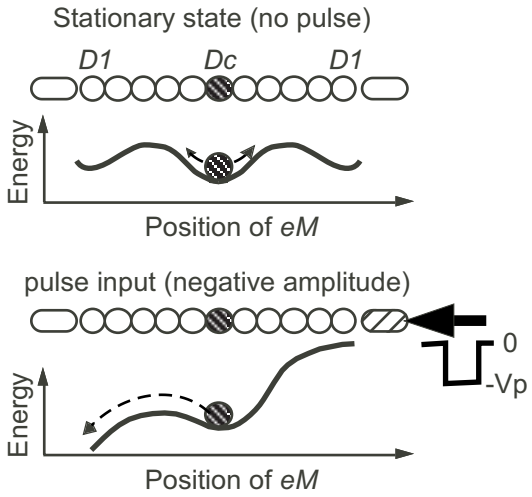

Fig. 3: Total energy profile in 1D nanodot array.

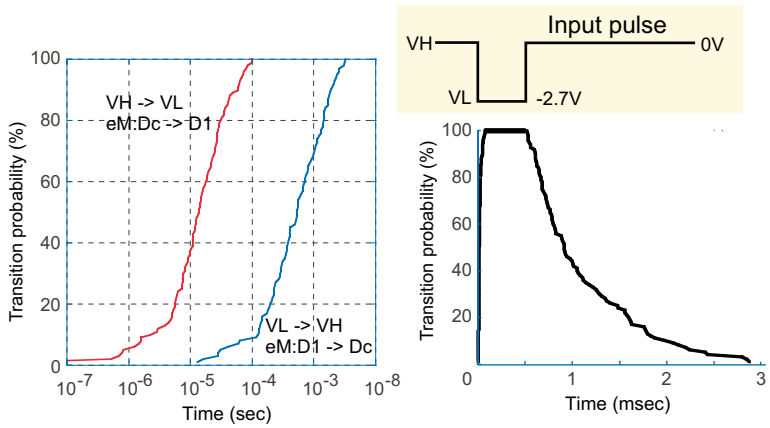

Fig. 4: Electron transition probability as a function of time.

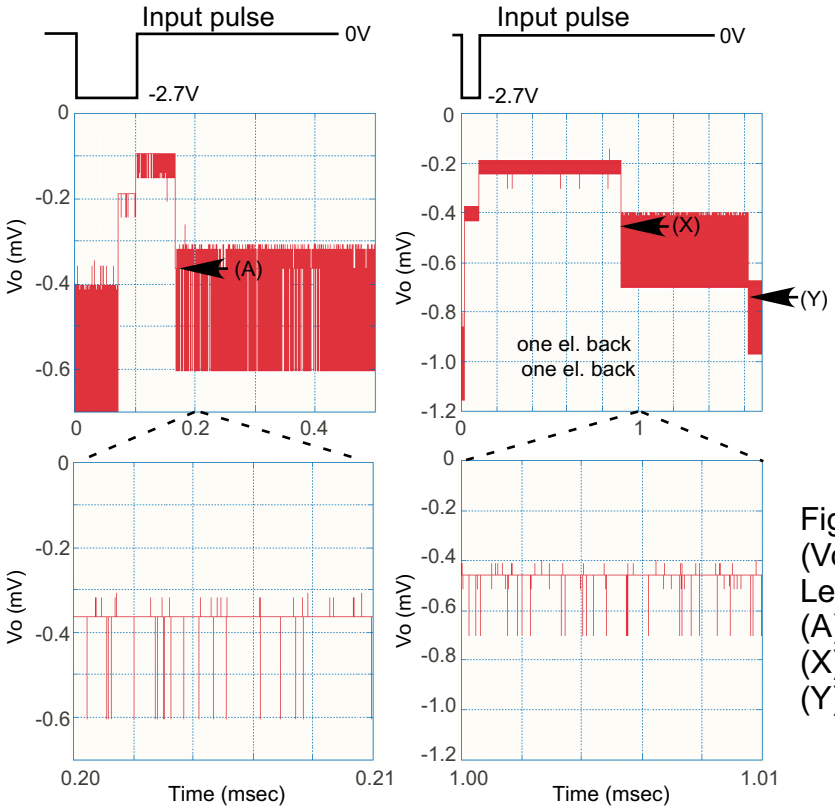

Fig. 5: Time dependence of MOS gate voltage (Vo).
Left: 1-input case, Right: 2-input case.
(A): the electron comes back to center dot (Dc).
(X): first electron comes back to Dc,
(Y): second electron comes back to Dc.