A Stochastic Association Circuit Using PWM Chaotic Signals

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1. Introduction

Associative memory is a basic function in intelligent information processing. Although the associative memory usually only extracts the pattern most similar to the input, it seems useful in some applications to know the information of similarities about several candidates. In the conventional associative memory architectures, additional complicated processing is required for obtaining such information.

We have already proposed new association circuit architectures utilizing stochastic behavior of single-electron transistors [1, 2]. They stochastically extract a stored pattern with a probability corresponding to the similarity. This is referred to as *stochastic association*. Repeating the association process, the similarity order of the promising candidates can be obtained.

In this paper, we propose a stochastic association circuit using chaotic signals and present a CMOS chip designed based on it.

2. Stochastic association circuit using chaos

In the stochastic association, the stored pattern most similar to the input is extracted with the highest probability; i.e., the most similar pattern is not always extracted, but the second most similar pattern is sometimes extracted, and the third is extracted with less probability.

All patterns processed in this circuit consist of N bit binary data, which are referred to as *words*, and the stored data consist of M words. The basic architecture is shown in Fig. 1. The input data is *stochastically* compared with each stored data by word-comparators (WC) in parallel. All WC's results are fed into the winner-take-all (WTA) circuit, and the largest result is extracted. In the circuit proposed here, the WC's results are represented by currents, and the WTA circuit operates in the current mode [3] as shown in Fig. 2.

Stochastic bit-level comparison between the input and stored patterns are performed in parallel by each bit-comparator (BC) in the WC as shown in Fig. 3. The BC consists of an exclusive-NOR (XNOR) gate, a PWM chaos generator (PCG), a latch, and a switched current source (SCS). Each bit of the input data is compared with the corresponding bit of the stored data by the XNOR gate, and only when both bits are the same, the output of the gate drives the PCG. The PCG outputs a synchronous PWM pulse with a random width. The PWM pulse is latched at a certain timing T_L. The latched result switches the SCS, and a constant current I flows into the summing line.

In a WC, if n bit-comparators are activated and if the latch timing is very close to the rise timing of the PWM pulse, the output current of the WC is nI. Since the WC's output is exactly proportional to the similarity between the input and the stored data, deterministic association is performed as in the conventional associative memory in this case. However, if the latch timing is far from the rise timing of the PWM pulse, some BC's output currents are zero even when the comparing results are "yes". In this case, the second candidate may be a winner. Thus, the stochastic association is approximately achieved, and the association probability distribution can be changed by changing the latch timing.

The PWM chaos generator used in the BC is a key component in this circuit. This can generate arbitrary chaotic PWM/PPM signals by supplying an arbitrary nonlinear voltage waveform as shown in Fig. 4. This circuit is based on the idea in which an arbitrary nonlinear input-output relationship is obtained by sampling the corresponding nonlinear voltage waveform using a PWM/PPM signal [4, 5].

3. Chip design

We designed a proof-of-concept CMOS chip using a 0.6 μm CMOS process (Fig. 5). It includes 20 WCs and 20 BCs. The chip size is 4.5 × 4.5 mm sq, and the area of a BC is 121 × 155 μm sq. The area of a chaos generator is still large (about 100 × 100 μm sq.), but if specific chaos is used, more compact design is possible.

4. Circuit simulation results

We confirmed the basic operation of the CMOS circuit using HSPICE simulation. As a simple example, we performed digit pattern association, where the chaotic signals were generated using the logistic map. The stored patterns consist of seven segments, and represent numbers 0,1,5,6. Since the ON/OFF state of each segment corresponds to a bit data, stored data are 4 words, each of which has 7 bits. Figure 6 shows two examples of the output of the WTA circuit; (a) the winner is "5", which is the same stored data as the input, and (b) the winner is "6", which is the second candidate. Figure 7 shows the difference of association distribution caused by changing the latch timing.

5. Conclusion

We proposed a CMOS circuit approximately performing stochastic association using chaotic signals. Since this can also simulate the stochastic behavior of single-electron devices, it could be used as a hardware emulator for future electronic systems using quantum structures.

Acknowledgments

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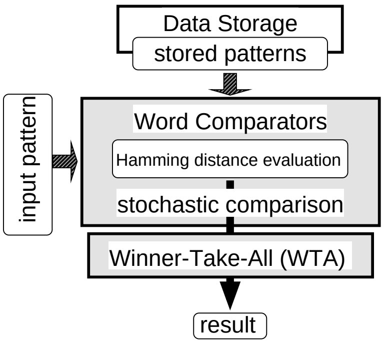

Figure 1: Stochastic association circuit architecture

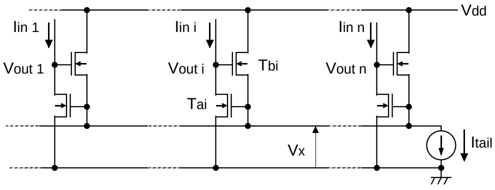

Figure 2: Winner Take All circuit

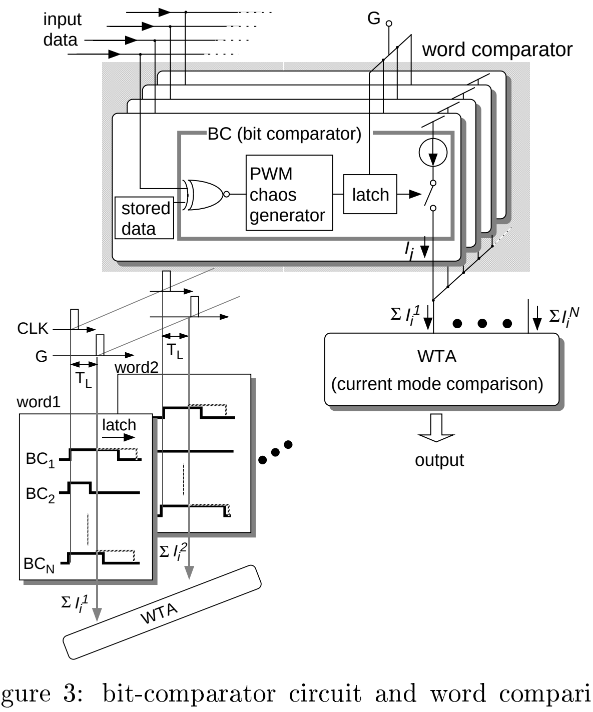

Figure 3: bit-comparator circuit and word comparison operation

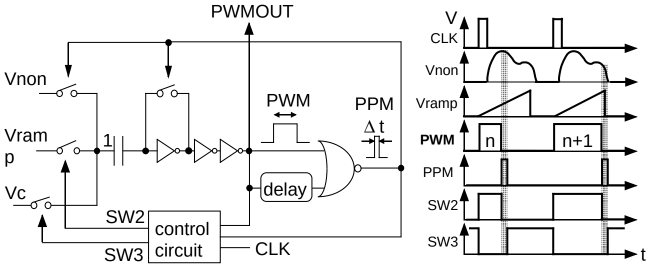

Figure 4: PWM chaos generator circuit

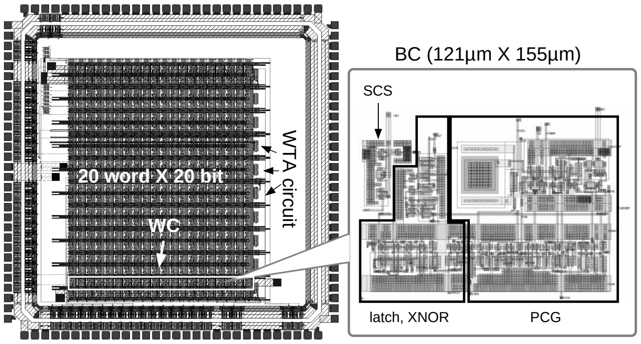

Figure 5: CMOS stochastic association chip layout

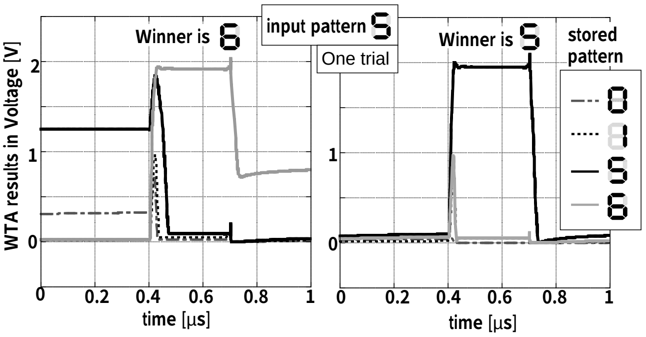

Figure 6: WTA output waveforms

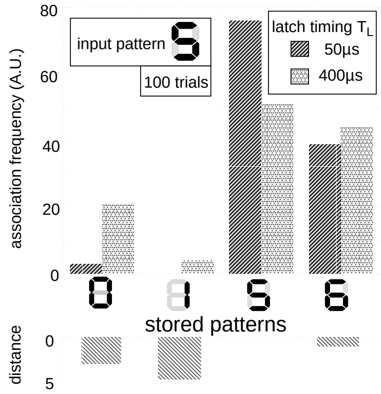

Figure 7: Association distribution