A Stochastic Associative Memory Using Single Electron Devices and its Application to Digit Pattern Association

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1. Introduction

Recently, extensive studies of single electron devices have been carried out, and many circuits using them have been actively proposed. Most of the proposed circuits are binary digital circuits which operate deterministically [1]. In some reports, however, applied circuits utilizing stochastic properties of single electron devices have been proposed [2]. An associative memory using the circuit proposed in Ref. [2] has also been proposed [3]. At the present stage, however, the configuration of this circuit is too complicated to confirm the operation by simulation.

In this paper we propose a new associative memory simpler than that in Ref. [3], and describe the simulation results using the Monte Carlo method [4]. We also demonstrate the new function of our memory by simulation of simple digit pattern association.

2. Associative Memory Architecture

An associative memory is usually defined as a device which extracts the pattern most similar to the input pattern from the stored reference patterns. When the pattern is represented by binary data, which we call a *word*, bit comparators for comparing input pattern bits with stored pattern bits are necessary for each word. The number of unmatched bits between the input data and the reference data is called the Hamming distance; the data having a shorter Hamming distance are considered to be more similar.

The associative memory that we propose in this paper consists of data storage, word comparators and a Winner Take All (WTA) circuit as shown in Fig. 1. The word comparator consists of bit-comparators (BCs) and evaluates the Hamming distance between the input pattern and the stored reference patterns. We apply single electron devices to the BCs, and attain stochastic association.

3. Basic Circuits and Operations

A single electron transistor (SET) [1] behaves as an exclusive-NOR (EXNOR) gate when the gate and sub-gate of SET are considered as two input terminals. In order to symmetrize the H-H and L-L outputs, the BC consists of two SETs that operate complementarily with each other. Figure 2 shows a schematic of the BC and the simulation results. The rising rate of voltage *Vco* changes slightly in every operation because electron tunneling events are stochastic.

The stochastic word comparator can be realized by connecting all nodes *Nc* of the BCs that correspond to all bits for the word with the common output capacitance *Co*. The number of BCs that can pass electrons through the junctions to the capacitance *Co* increases as the Hamming distance between the two patterns to be compared becomes shorter. However, the output voltage when the Hamming distance is the shortest does not always increase most rapidly due to stochastic tunneling events.

The WTA circuit selects the word comparator output reaching the threshold voltage first (Fig. 3). Because the output capacitance *Co* is large enough (~0.5fF), the BC outputs can be connected to sub 100nm MOS devices (*Cox*<1fF) without serious effects on the SET circuit operation. Thus, we assume that the WTA circuit consists of CMOS circuits, and that it works ideally in the following simulation.

We also assume that the reference data are supplied from outside and that word comparators can read reference data from the data storage at any time in parallel.

4. Simulation results

We confirmed the basic operation of the associative memory by simulation of simple digit pattern association. The stored patterns consist of seven segments, and can represent numbers 0,1,...,9. Because the ON/OFF state of each segment corresponds to a bit data, stored data are 10 vectors, each of which has 7 binary elements. An example of output voltage changes in the word comparators is shown in Fig. 4. Figure 5(a) shows association frequencies in all reference patterns when the input digit pattern is “5”, where the association is repeated 100 times. Figure 5(b) also shows those when the input pattern is not included in the stored reference patterns. Both simulation results show the association probability increases as the Hamming distance from the input pattern becomes shorter. Repeating the stochastic association, pattern similarity order (order in Hamming distance) can be obtained. This is the unique feature of this device, which is difficult for ordinary deterministic associative memory devices to obtain.

5. Conclusion

The proposed stochastic associative memory using the unique property of single electron devices associates a more similar pattern with a higher probability. We confirmed the basic circuit operation by Monte Carlo simulation.

Acknowledgment

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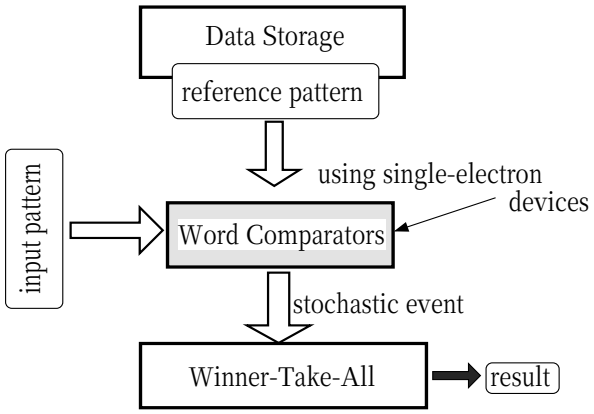


Fig. 1 Associative memory architecture.

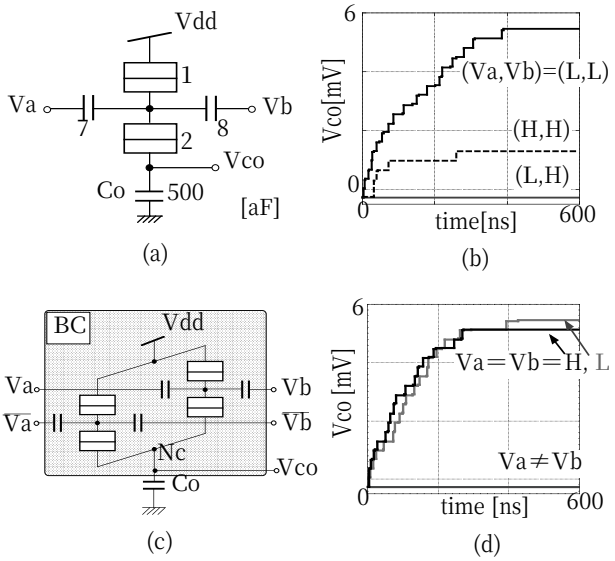


Fig. 2 Schematic of single electron transistor (SET) (a) and the simulation results (b). Bit comparator (BC) (c) and the simulation results (d).

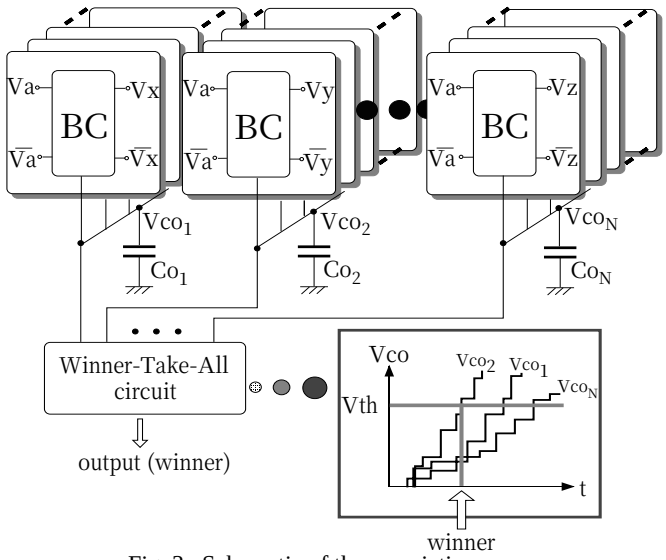


Fig. 3 Schematic of the associative memory.

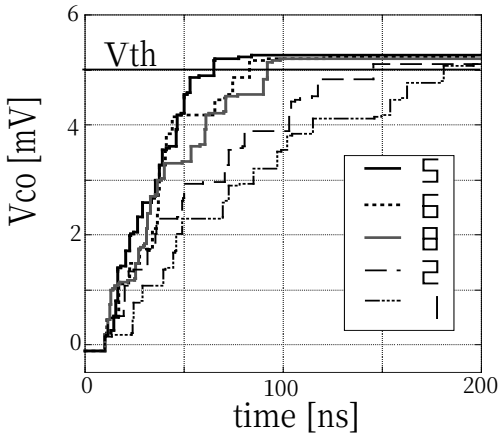
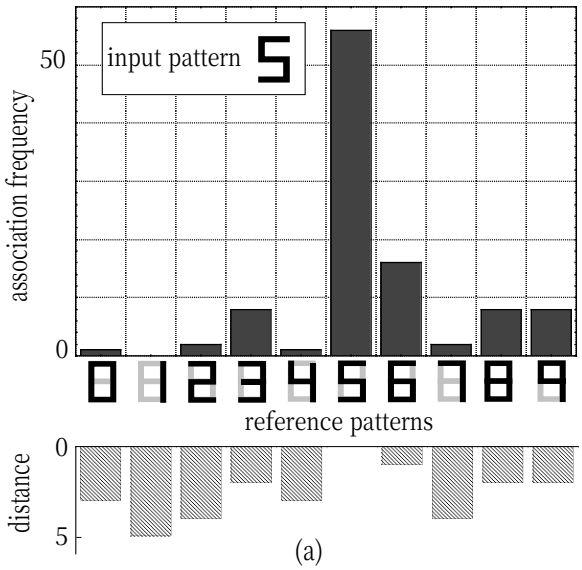


Fig. 4 An example of voltage changes in the word comparators. The threshold voltage (Vth) is 5[mV]. In this case, the winner is “5”, but in the next association, the winner may be different.



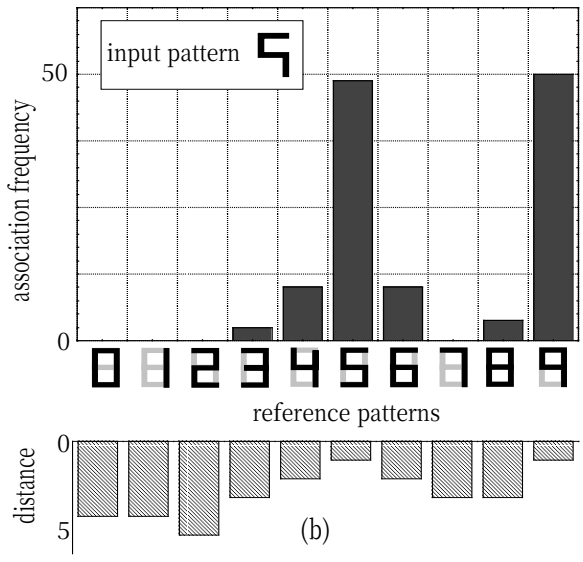


Fig. 5 Association frequency for each stored pattern when the operations are repeated 100 times. (a)The input pattern is "5". (b)The input pattern is not included in the stored patterns.