A 1-D CMOS PWM Cellular Neural Network Circuit and Resistive-Fuse Network Operation

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1. Introduction

The resistive-fuse network is a well-known image segmentation processing model in which image edges are preserved and noise is eliminated. Some attempts for its analog LSI implementation have been proposed [1]. Although the analog approach achieves compact circuit size and fast processing speed, a practical design for large-scale resistive-fuse network circuits (more than 100 $\times$ 100 pixels) is very difficult to realize because of unexpected parasitic components and various disturbances such as noise, interference, and device parameter mismatch.

To overcome these difficulties, we have already proposed pulse-width-modulation cellular neural network (PWM-CNN) circuits, which can implement the resistive-fuse network model with high controllability. [2, 3].

In this paper, we propose an efficient subtraction circuit for the PWM-CNNs, and describe the design result of a 1-D CMOS PWM-CNN LSI chip. We also demonstrate the resistive-fuse network operation using a fabricated PWM-CNN chip.

2. Resistive-Fuse Networks with Discrete-Time Dynamics

Figure 1 shows a circuit diagram of the resistive-fuse network in which resistive-fuse elements connect the pixel nodes. The image input I_n for pixel n is given as a voltage source. The processing result (output) O_n is given as a node voltage. If the difference between neighboring pixels $|O_n - O_k|$ is smaller than the threshold value δ, the network behaves as a simple linear resistive network, and image smoothing is performed. On the other hand, if $|O_n - O_k| \geq \delta$, the pixel nodes are disconnected each other, and such pixels are recognized as an image edge.

Our PWM-CNN emulates the operation of this circuit by discrete-time dynamics based on clock operation. The change in each node voltage is calculated using Kirchhoff's law, and the steady state is obtained by repeating the updating process.

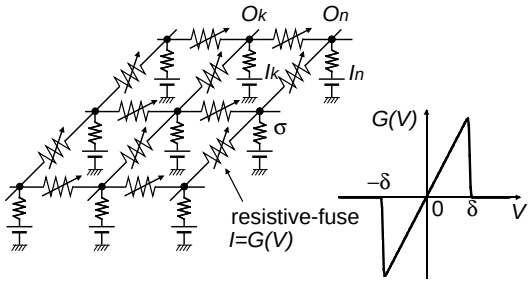

Fig. 1: Resistive-fuse network circuit

The dynamics is expressed as follows:

$$O_n(t+1) - O_n(t) = \nu[\sum_{k \in N_n} G(O_k - O_n) + \sigma(I_n - O_n)] \quad (1)$$

where N_n represents neighbor cells of n; ν and σ are constants. $G(\cdot)$ is a voltage-current characteristic of a resistive-fuse, as shown in Fig. 1. Because each term of the right side of Eq. 1 is expressed by an odd function of the difference of two values, the absolute value and the sign of the difference can be used.

3. A PWM Pixel Unit Circuit

A pixel unit circuit of PWM-CNN is shown in Fig. 2. The input I_n and output O_n are temporarily stored at capacitors C_{In} and C_{On}, respectively.

The updating process proceeds as follows:

1) Selector *SEL* selects a set of signals to be calculated, which corresponds to one term on the right side of Eq. 1.
2) The absolute value and the sign of the difference between the two signals such as $(O_k - O_n)$ or $(I_n - O_n)$ are calculated by subtraction circuit *SUB*. The circuit diagram of *SUB* and the timing diagram for subtraction are also shown in Fig. 2. At first, *SUB* does not know which input is larger. Therefore, at the first part of the operation, *SUB* performs subtraction for checking the sign. After obtaining the correct sign, the second subtraction is performed for generating PWM output.
   The sign bit determines whether the positive or negative updating of O_n is performed.
3) A PWM pulse whose pulse width corresponds to the absolute value of the difference switches the voltage source V_{non} whose voltage waveform in the time domain is the same as the corresponding function ($G(\cdot)$ or linear). Thus, capacitor C_3 holds the value of the corresponding term in Eq. 1.
4) The voltage stored in capacitor C_3 is again converted into a PWM pulse by comparing with V_{ramp2}, and it switches the current source I_+ or I_-. Output O_n is thus updated by the corresponding term.
5) Repeating the above processes, O_n is updated by another term.

4. A Fabricated Chip and Measurement Results

We designed a 1-D 20-pixel PWM-CNN circuit using 0.6μm CMOS technology. The layout image of the pixel unit circuit and a photograph of the fabricated chip are shown in Fig. 3. Each pixel has two unit circuits because this chip was designed so that it also works as a Gabor-filter circuit [2]. The

supply voltage was 3.3 V, and the power consumption was 33 μW per pixel unit circuit.

The measurement results are shown in Fig. 4. When a linear ramp waveform is given for generating $G(\cdot)$ (Fig. 4(a)), the circuit works as a linear resistive network. The whole image is smoothed and no edge is preserved. On the other hand, when the resistive-fuse characteristic is implemented (Fig. 4(b)), the network can successfully eliminate noise and preserve the edges simultaneously.

5. Conclusion

The proposed PWM pixel unit circuit serially implements the discrete-time dynamics of CNNs while it spatially performs pixel-parallel operation. Although the PWM approach requires more time to reach steady states than does the pure analog approach, it should provide much greater controllability and robustness because it numerically solves the dynamics by using analog pulse widths.

We successfully designed and fabricated a 1-D 20-pixel PWM-CNN circuit using 0.6μm CMOS technology. The next target is design of 2-D PWM-CNN circuits for real-time real-world image segmentation.

Acknowledgments

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References

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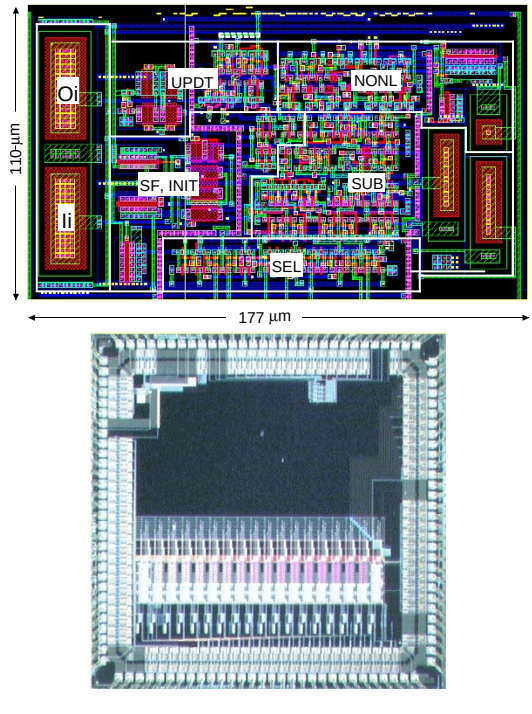

Fig. 3: Pixel unit circuit layout and micro-photograph of the PWM-CNN chip (die size: 4.6mm sq.)

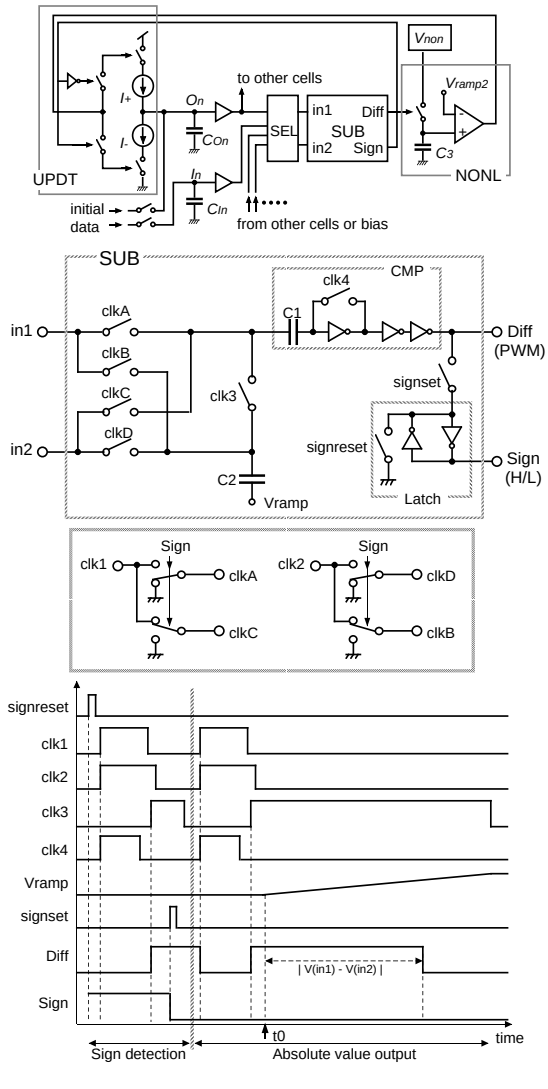

Fig. 2: Pixel unit circuit and timing diagram for subtraction operation. Voltage waveform $V(non)$ starts at t_0.

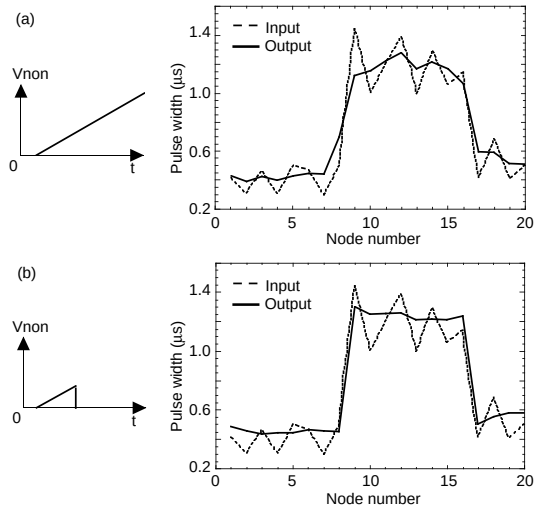

Fig. 4: Measurement results of a 1-D resistive-fuse network. The number of updating iteration was 30, and the total operation time was 250μs.