Quantum Dot Structures Measuring Hamming Distance for Associative Memories

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Abstract

Two types of quantum dot circuits measuring a Hamming distance using the Coulomb repulsion effect are proposed and analyzed. They have structures where a quantum dot array is arranged on a gate electrode of an ultrasmall MOSFET. The device parameters for successful operation are clarified from Monte-Carlo simulation.

KEYWORDS: Quantum dots, Single electron devices, Coulomb repulsion, Hamming distance, Associative memory

1. Introduction

Single-electron devices have intrinsic difficulties from a viewpoint of system applications: slow operation speed and insufficient reliability [1] due to stochastic tunneling events and serious background charge sensitivity [2]. Thus, the conventional multi-stage digital circuit architecture is not suitable for single-electron devices.

In our strategy for constructing single-electron circuits, single-electron devices are used for repeatable circuits with a few logic-stages, and ultrasmall CMOS devices are used for multi-stage logic circuits. The above-mentioned difficulties are overcome by massively parallel operation and redundant architecture by virtue of very large packing density and very low power dissipation of single-electron devices.

In this paper, as an example of such circuits, we propose two functional circuits using the Coulomb repulsion effect between quantum dots. These circuits measure the Hamming distance, the number of the unmatched bits between two digital data, which are a core circuit for associative memories. Although such circuits using single-electron transistors have already been proposed [3, 4], the circuits using quantum dots have advantages of achieving static operation and robustness to fluctuation of device parameters such as the tunneling resistance.

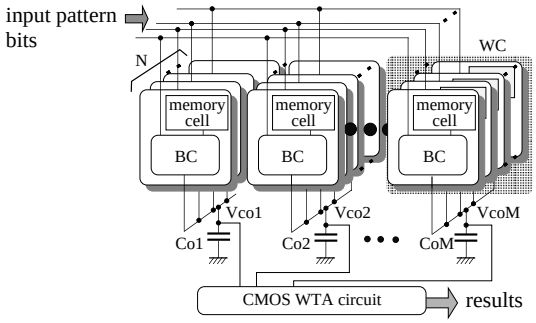

Figure 1: Associative memory architecture.

2. Associative memory architecture using quantum dots and ultra-small CMOS devices

The associative memory assumed here compares the input pattern with the stored patterns, and extracts the pattern most similar to the input. We assume that each pattern consists of N bit binary data, which is referred to as a *word*, and the stored data consist of M words. The similarity between digital data is usually measured by a Hamming distance.

As shown in Fig. 1, bit-level comparison between the input data and each stored data is performed by each bit-comparator (BC) in a word-comparator (WC) in parallel. The WC calculates the Hamming distance between the input data and the stored data by collecting the results of the BCs; that is, the comparison result is expressed as the number of electrons released from the BCs, and the electrons are collected at the capacitor $C_{oi}, i = 1, \cdots, M$. All WC's results are fed into the winner-take-all (WTA) circuit, and it extracts the stored word data that has the shortest Hamming distance.

We assume the WTA circuit is constructed using CMOS devices, and propose two quantum dot circuits for the WC in the next section.

3. Quantum dot circuits measuring Hamming distance

Let us assume a string of quantum dots as shown in Fig. 2(a), put an electron, e_M, at one of the three dots D_1, and represent a bit (0 or 1) of the input and stored data by whether an electron is put at each end dot D_2 or not. When the corresponding bits of both data are matched, because Coulomb repulsion is symmetric, electron e_M is stabilized at the center; otherwise it is off-center. In order to detect the position of electron e_M, two detection circuits are proposed: circuit-A that detects the center position and circuit-B that detects the off-center position as shown in Figs. 2(b) and (c). By the Coulomb repulsion effect, the bit matching result reflects whether electron e_R tunnels to node N_o. Consequently, electrons whose number is equal to that of the matched bits (circuit-A) or that of the unmatched bits (circuit-B) are accumulated in C_o. To ensure the stabilizing processes, control voltage V_g are used.

A 3-D arrangement of quantum dots realizing circuit-A is shown in Fig. 3, where

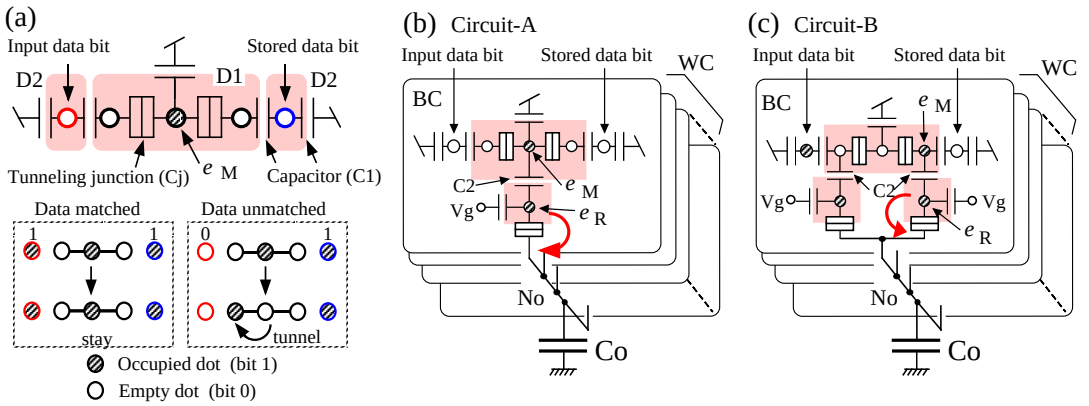

Figure 2: Principle of bit-comparison using Coulomb repulsion effect (a), and two word-comparator circuits (b)(c).

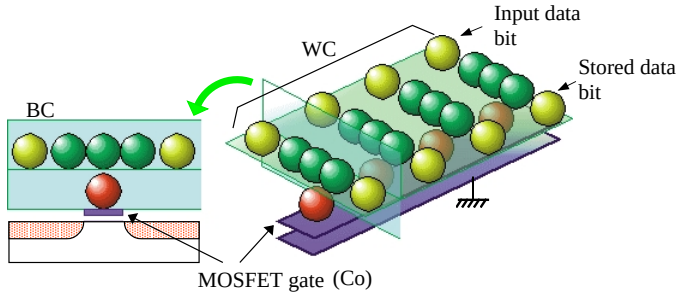

Figure 3: 3-D structure image of a word-comparator (Circuit-A).

common terminals to the ground and control voltages are omitted. The capacitance C_o corresponds to the gate capacitance of an ultrasmall CMOS transistor.

In this architecture, if it is difficult to represent one bit by one quantum dot, we can use a redundant architecture where plural BCs represent one data bit. Such an architecture based on a majority decision principle has an advantages of robustness against effects of background charge.

4. Circuit simulation results

We analyzed the proposed circuits by Monte Carlo single-electron circuit simulation, where parasitic capacitance between ground and quantum dots, C_g, and that between the second-neighbor quantum dots, C_d are considered. We found that circuits A and B have almost the same characteristics. Because the structure of circuit-A is simpler than that of circuit-B, we only describe here the simulation results for circuit-A.

The operation temperature ranges for feasible capacitance values are shown in Fig. 4(a). The upper limit of operation temperature gradually lowers with increasing C_g and C_d. In order to operate the circuit at higher temperature, one has to scale

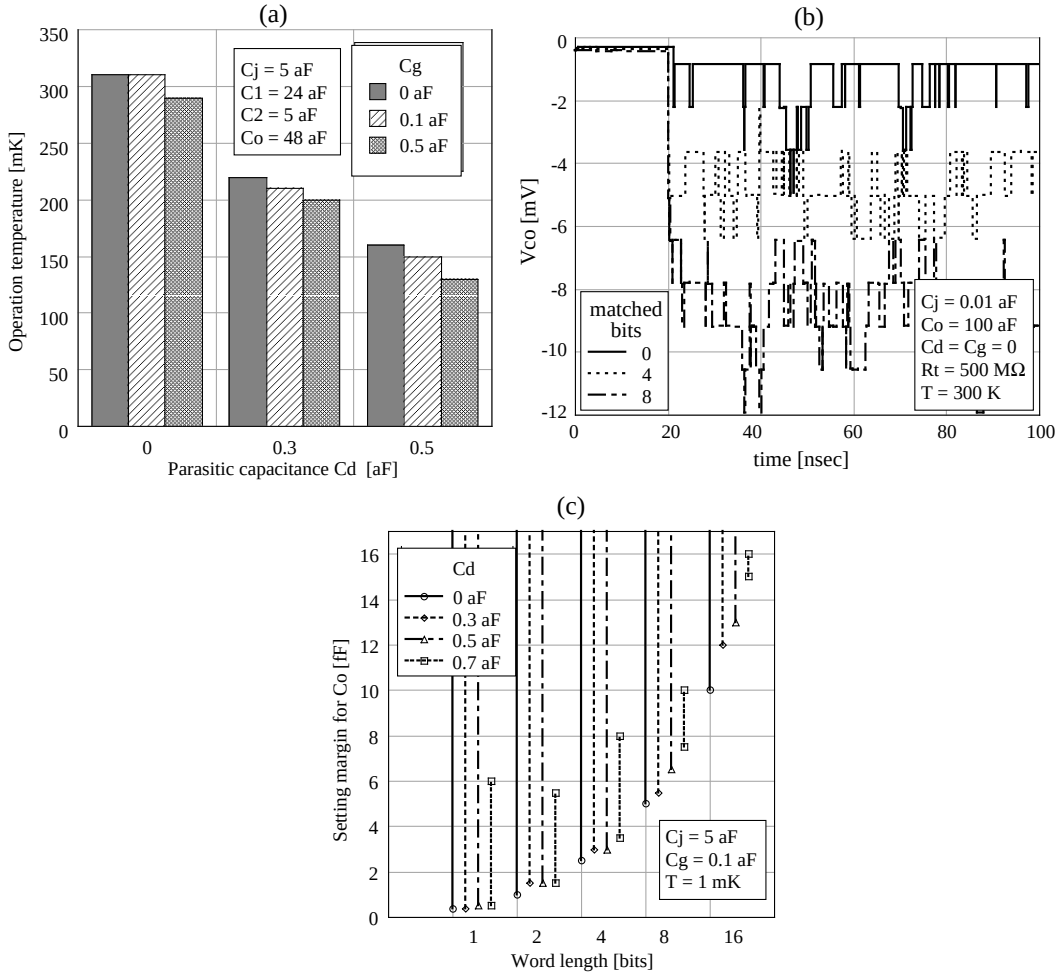

Figure 4: Simulation results for circuit-A: (a) operation temperature range with one BC, (b) output voltage changes at room temperature, and (c) setting margin for C_o.

down all the values of capacitance, and at the same time, scale up the applied voltages. For room temperature operation, tunnel junction capacitance of 0.01 aF is required as shown in Fig. 4(b) although this value is very difficult to realize.

Setting margin of C_o is shown in Fig. 4(c) as a function of the word length (the number of the connected BCs). There exist minimum values of C_o for the correct operation, and the values increase as the word length increases. This is because some electrons e_R cannot tunnel to node N_o because of the Coulomb blockade effect by other e_R's. If the parasitic capacitance is negligible, there do not exist the upper limits of C_o. However, C_o should be as small as possible because the sensitivity to one electron in the output voltage e/C_o decreases with increasing C_o.

5. Conclusion

The proposed quantum dot structures can be realized in the near future because they are similar to floating-gate quantum-dot memory devices that have already been fabricated. However, well-controlled self-organization technologies should be developed.

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