Quantum Dot Structures Measuring Hamming Distance for Associative Memories

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ABSTRACT

This paper describes new quantum-dot circuits that measure a Hamming distance by using the Coulomb repulsion effect between quantum dots. Measuring similarity between patterns expressed by a Hamming distance is a basic function for various information processing. Quantum dot structures realizing these circuits are also proposed, which will be constructed by using the well-controlled nanocrystalline floating-dot MOSFET technology. For room temperature operation, the simple quantum-dot circuit requires a tunnel junction capacitance of less than 0.01 aF, but the multi-quantum-dot circuit using thermal-assisted tunneling allows to use the capacitance of up to 0.1 aF. This technique is useful for designing practical single-electron circuits performing intelligent information processing.

1. Introduction

Single-electron devices are intrinsically problematic from the viewpoint of system applications; they are burdened by slow operation speed and insufficient reliability [1] due to stochastic tunneling events and serious background charge sensitivity [2]. Thus, conventional multi-stage digital circuit architecture cannot be applied to single-electron devices. New single-electron circuits based on new information processing principles need to be developed.

Our strategy for constructing single-electron circuits combines the use of single-electron devices for repeatable circuits with a few logic-stages and ultrasmall CMOS devices for multi-stage logic circuits. Large capacitance is used as an interface between the two devices. The intrinsic difficulties mentioned above are overcome by massively parallel operation and redundant architecture made possible by the very high packing density and very low power dissipation of single-electron devices.

In order to utilize a unique stochastic feature of single-electron operation, a new information processing principle called *stochastic association* has been proposed [3, 4]. Meanwhile, we have proposed some single-electron circuits based on the aforementioned strategy that measure the Hamming distance, the similarity between two data. This is a basic function not only for associative memory but also for matching circuits used in various information processing such as image recognition and data compression. These circuits employ the Coulomb blockade effect in single-electron transistors (SETs) [3, 4, 5] or the Coulomb repulsion effect and thermal-assisted tunneling between quantum dots [6, 7]. These circuits will be realized by using the well-controlled nanocrystalline floating-dot MOSFET technology, which is being actively studied for use in future memory devices [8, 9].

We have also designed a CMOS stochastic associative processing chip using chaotic signals, which can also be used as an emulator system for single-electron circuits [10].

This paper will focus on quantum-dot circuits that employ the Coulomb repulsion effect. First, the circuit architecture, comprised of quantum-dots and ultrasmall MOSFETs, will be described. Next, a simple quantum-dot circuit measuring a Hamming distance will be presented and its characteristics discussed. Finally, a multi-quantum-dot circuit for room temperature operation will be described. It utilizes thermal-noise assisted tunneling, a new approach in single-electron devices that allows an increase in operating temperature.

2. Associative memory architecture using quantum dots and ultrasmall CMOS devices

The associative memory assumed here compares the input pattern with the stored patterns, and extracts the pattern most similar to the input. We assume that each pattern consists of N bit binary data, which is referred to

as a *word*, and the stored data consist of M words ($N, M \gg 1$). The similarity between digital data is measured by a Hamming distance, that is the number of the unmatched bits between two data.

As shown in Fig. 1, bit-level comparison between the input and each stored pattern is performed by each single-electron bit-comparator (BC) in a word-comparator (WC) in parallel. The WC calculates the Hamming distance between the input data and the stored data by collecting the results of the BCs; that is, the comparison result is expressed as the number of electrons released from the BCs, and the electrons are collected at capacitor $C_{oi}, i = 1, \cdots, M$. All WC's results are fed into the winner-take-all (WTA) circuit, and it extracts the stored word data that has the shortest Hamming distance. We assume the WTA circuit is constructed using CMOS devices because the size of the WTA circuit is much (N-times) larger than the single-electron BC. In the following sections, we propose two quantum-dot circuits for the WC.

3. Quantum dot circuits measuring Hamming distance

Let us assume a one-dimensional (1-D) array of quantum dots as shown in Fig. 2(a), put an electron, e_M, at the center dot D_c, and represent a bit (1 or 0) of the input and stored data by whether an electron is put at each end dot D_e or not. When the corresponding bits of both data are matched, because Coulomb repulsion is symmetric, electron e_M is stabilized at D_c; otherwise it is at one of off-center dots D_o. This bit matching result reflects whether electron e_R tunnels to node N_o, as shown in Fig. 2(b). Consequently, electrons whose number is equal to that of the matched bits are accumulated in C_o.

A 3-D arrangement of quantum dots realizing this WC circuit is shown in Fig. 3. The capacitance C_o corresponds to the gate capacitance of an ultrasmall CMOS transistor. This structure will be fabricated by the technology of nanocrystalline floating-dot MOSFET devices [8, 9].

In this architecture, if it is difficult to represent one bit by one quantum dot, we can use a redundant architecture where plural BCs represent one data bit. Such an architecture based on a majority decision principle has an advantages of robustness against effects of background charge.

We analyzed the proposed circuit by Monte Carlo single-electron circuit simulation. Figure 4 shows voltage changes at node N_o for various Hamming distances (D_H) at room temperature, where tunnel junction capacitance $C_j = 0.01$ aF. The results show that we can manage to discriminate the difference of D_H. However, very small C_j (0.01 aF) is required for room temperature operation. This is because the total energy is directly related to C_j, as in all of the previously reported single-electron circuits. This value is very difficult to realize by using near future technology, and quantum effects that are not considered in our simulation emerge in such a small junction capacitance region. Therefore, we have to develop new circuits that operate properly with C_j of at least 0.1 aF. In the next section, we propose such a new circuit.

4. A multi-quantum-dot circuit using thermal-noise assisted tunneling

We propose a new circuit and structure using tunneling processes assisted by thermal noise. In the new circuit, additional dots are inserted between D_c and D_o, and between D_c and N_o as shown in Fig. 5. By applying appropriate bias voltages, the profile of the total energy in the 1-D dot array structure ($D_e, D_o, \cdots, D_c, \cdots, D_o, D_e$) as a function of the position of e_M has two peaks at the additional dots, and has minimal values at D_c and both of D_o as shown in Fig. 6. For *1-1 state*, where electrons are put at both D_e, the energy at D_o rises up, thus e_M is most strongly stabilized at the center position. Therefore, the difference between *0-0 state* and *0-1(or 1-0) state* has to be considered for obtaining the proper operating condition. Figure 6 also shows the precise energy profile obtained by the simulation where C_j is 0.1 aF; tunnel resistance R_t is 5 MΩ; operation temperature is 300K. The energy barrier height for e_M at D_c is larger than the thermal energy at room temperature.

Because the energy barrier height in *0-1(1-0) states* is lower than that in *0-0 state*, there exists a certain time span t_0 within which e_M in *0-1(1-0) states* reaches D_o due to thermal noise, while e_M in *0-0 state* stays at the center position. Figure 7 shows the relation between operation temperature and time required until e_M reaches D_o. At room temperature (300K), t_0 is several microseconds in this case although t_0 depends on R_t.

Figure 8 shows voltage changes at node N_o for various Hamming distances at room temperature, where the voltage for a distance of 0 bit was considered to be 0 V. The voltage changes are proportional to the Hamming distance, and larger than 1 mV, which is the lowest value to detect with an MOSFET. Thus, it was confirmed

that the new circuit can operate at room temperature for the junction capacitance 10 times larger than that in the simple quantum-dot circuit described in the previous section.

5. Conclusion

In electronic information processing systems, CMOS ULSI will continue to be a major player for at least another decade. Therefore, single-electron devices and circuits that can be used with CMOS ULSI should be developed. Here, we propose several examples of such single-electron circuits and structures that possess new basic information processing functions. In order to fully realize the proposed quantum-dot structures, existing technology used in nanocrystalline floating-dot memory devices can be employed, but well-controlled self-assembly techniques must be developed.

The proposed new operation principle using thermal noise seems to be similar to a phenomenon known as *stochastic resonance*, which plays an important role in biological neural systems. Imitation of biological systems promises to be an important tool in developing various single-electron circuits performing intelligent information processing utilizing noise or fluctuation.

Acknowledgments

The authors wish to thank Prof. Masataka Hirose for his support. This work has been supported by the Core Research for Evolutional Science and Technology (CREST) from Japan Science and Technology Corporation (JST).

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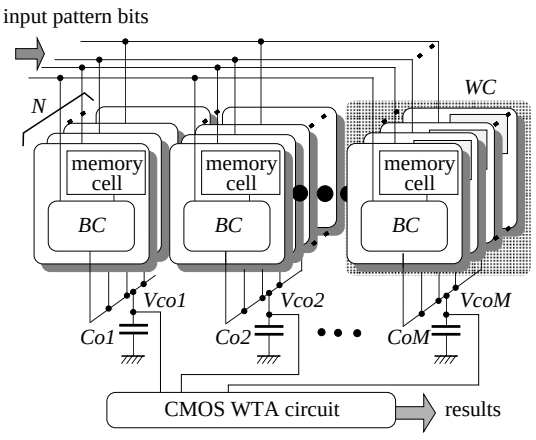

Fig. 1: Associative memory architecture.

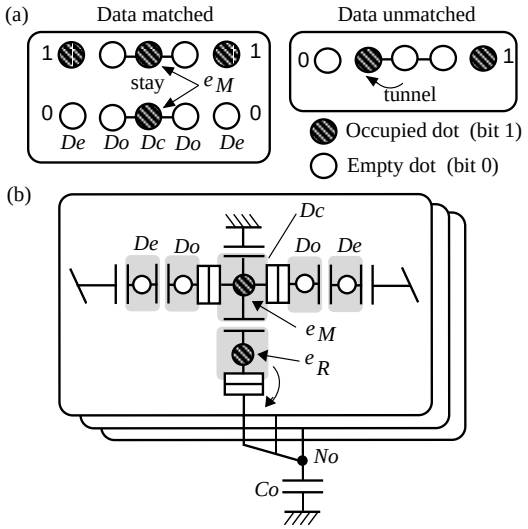

Fig. 2: Principle of bit-comparison using Coulomb repulsion effect (a) and bit-comparator circuit (b).

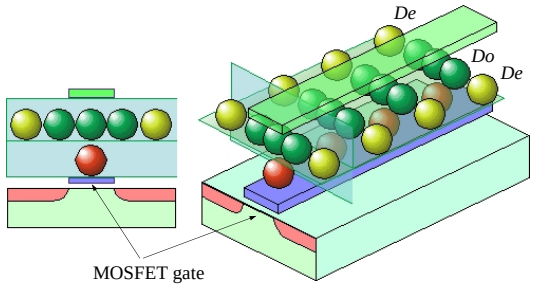

Fig. 3: 3-D structure image of a word-comparator.

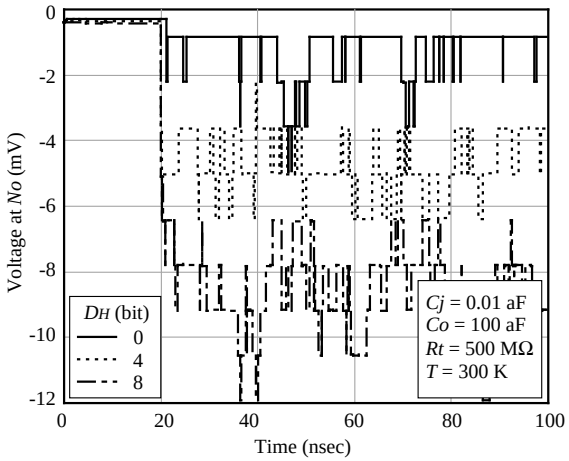

Fig. 4: Voltage changes at node N_o for various Hamming distances (D_H) in the circuit shown in Fig. 2.

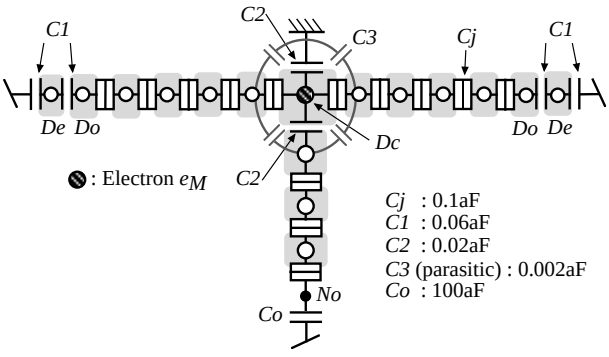

Fig. 5: A multi-quantum-dot circuit and the parameter values used in the simulation.

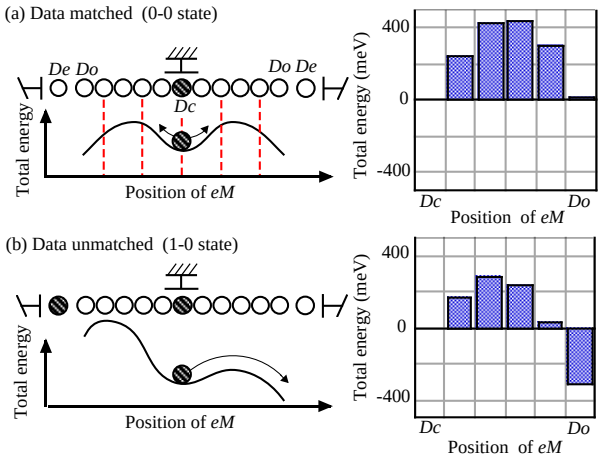

Fig. 6: Total energy profile of 1-D dot-array structure and its simulation results.

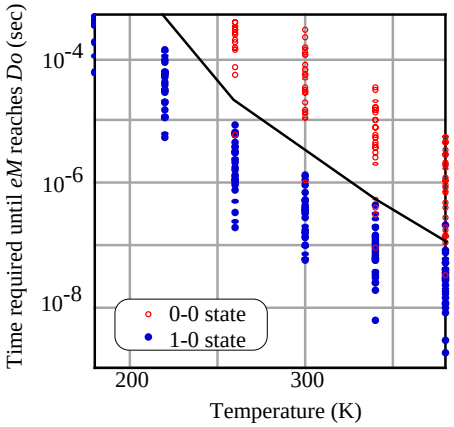

Fig. 7: Relation between operation temperature and time required until e_M reaches D_o. The solid line indicates t_0.

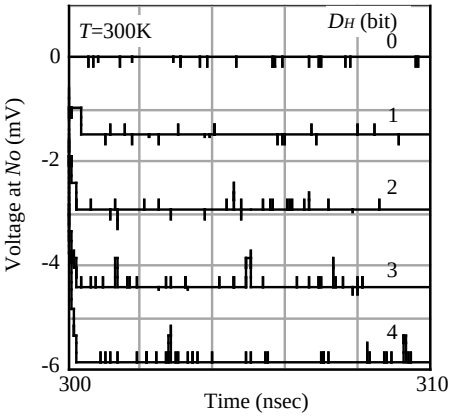

Fig. 8: Voltage changes at node N_o for various Hamming distances (D_H) in the multi-quantum-dot circuit.