DESIGN OF A PIXEL-PARALLEL FEATURE EXTRACTION VLSI SYSTEM FOR BIOLOGICALLY-INSPIRED OBJECT RECOGNITION METHODS

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Abstract—

This paper proposes a biologically-inspired feature extraction method, which consists of coarse region segmentation by a resistive-fuse network and feature extraction by Gabor wavelet transforms. Their pixel-parallel VLSI implementation based on the pulse modulation circuit architecture is described, and measurement results of Gabor filter operation by a test LSI chip with 1-D 20-pixels are presented.

I. INTRODUCTION

Beyond the *Silicon retina* [1], in order to mimic the functions of the primary visual cortex, simple feature extraction by Gabor wavelet transforms should be implemented first, which extract specific spatial frequency components with given directions. In the brain, these transforms are performed by the simple cortical cells, and massively parallel processing is achieved in hypercolumn structures.

However, it is very difficult for present VLSIs to perform massively parallel processing with 3-D matrix structures and interconnections as in the hypercolumn. This situation is different from the case of retina, which roughly has a 2-D structure. Fabrication technology for 3-D VLSIs is being developed [2], but it can construct at most several-layer structures.

In this paper, first, we propose a feature extraction method suitable for the present 2-D structure VLSIs. In the proposed method, first, coarse region segmentation is performed, where small shades are ignored, and then each segmented region is extracted, and Gabor wavelet transforms are performed for each extracted region. We briefly describe the pixel-parallel VLSI implementation based on our pulse modulation circuit architecture. We focus on the VLSI implementation of Gabor wavelet transforms, and describe the results of design and measurement of a test LSI chip for 1-D Gabor filters.

II. DESIGN OF A FEATURE EXTRACTION VLSI SYSTEM

A. Pixel-parallel VLSI implementation

In order to perform information processing in 3-D structures by 2-D VLSIs, time-division processing should be introduced. We adopt a pixel-parallel architecture, which has a 2-D processing unit array corresponding to the pixel array. This approach is promising because it will make high-functional vision chips by integrating on-chip image sensors.

Because the ordinary digital circuit approach requires large circuit area, it is difficult to adopt pixel-parallel architecture. In contrast, the analog circuit approach makes circuit size compact, but from the viewpoint of calculation precision and controllability, large scale integration of the pixel units is difficult.

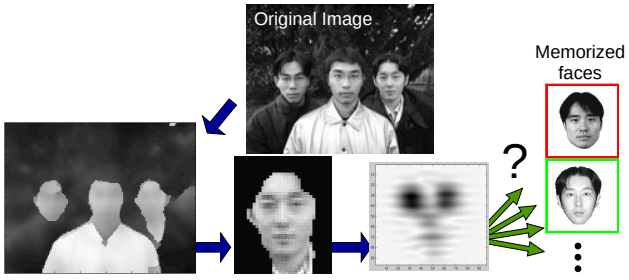
We have proposed a pulse modulation circuit architecture, which has advantages of both digital and analog approaches [3, 4]. However, even when this architecture is used, we can only design a VLSI chip with at most 100×100 pixels by using the present VLSI technology. In order to process natural scene images with megapixels, introducing a segmentation process is inevitable.

B. Feature extraction scheme with image segmentation

As biologically-inspired models for image recognition, hierarchical architectures for integrating local features have been proposed; e.g. Neocognitron [5]. However, this type of architecture requires large amount of hardware resources.

Here, we do not adopt such architecture. Instead, we propose a combination of coarse region segmentation and feature extraction in each segmented region, which is a realistic solution for present VLSI systems.

In this approach, the original image should be segmented into recognition target objects, and each object is processed for recognition. However, precise segmentation requires the recognition result of the whole image, but it cannot be obtained before segmentation. To solve this dilemma, we temporarily segment the image by using brightness of local



Function	Image Segmentation	Region Extraction	Feature Extraction
Model	Resistive-fuse Network	Oscillator Network, Cellular Automaton	Cellular Neural Network
Output	edge data	extracted area	Gabor wavelet

Figure 1: Feature extraction process of natural scene images. The target object is human faces.

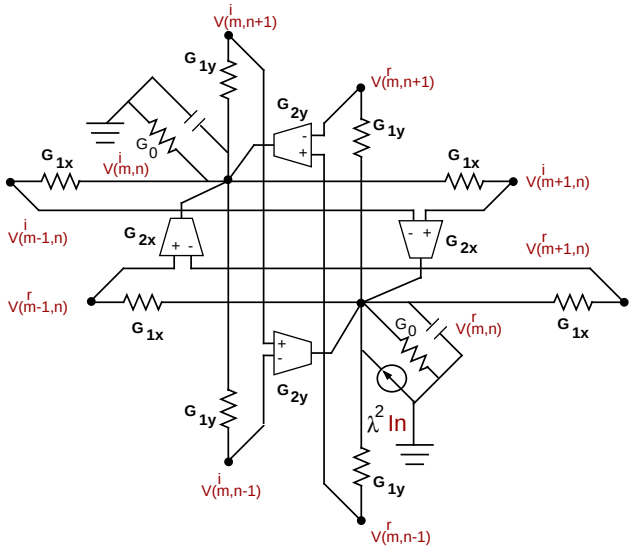


Figure 2: 2-D CNN circuit performing Gabor-type filtering, where I_n is the input for node n; $\lambda^2 = G_0 + 2G_{1x} + 2G_{1y} - 2(G_{1x}^2 + G_{2x}^2)^{1/2} - 2(G_{1y}^2 + G_{2y}^2)^{1/2}$, $G_{2x}/G_{1x} = \tan\omega_{0x}$, $G_{2y}/G_{1y} = \tan\omega_{0y}$.

area, and then try to recognize the segmented region. If a meaningful result is obtained, we realize that the segmentation succeeded. If not, we redo the segmentation process with different parameters.

Figure 1 shows the proposed feature extraction process. The target object is human faces in this case.

1) By using the resistive-fuse network, a gray-level natural scene image is segmented into some regions in each of which the pixels have nearly the same brightness regardless of small parts [6]. For example, whole face regions are segmented so that small parts such as eyes, brows, a nose, a mouth are eliminated.
2) Each segmented region is extracted one by one. For this process, the nonlinear oscillator networks called LEGION can be used [7], and we are also developing a cellular-automaton-type region extraction method, which can be implemented by digital circuits.
3) Feature extraction is performed for the extracted regions by using Gabor wavelet transforms.
4) The obtained Gabor coefficients are used for the object recognition process.

Since the details of the resistive-fuse networks and the oscillator networks are described in our other papers [6, 7], the rest of this paper describes VLSI implementation of the Gabor-filter.

III. PIXEL-PARALLEL GABOR-TYPE FILTER CIRCUIT

A. Analog circuit for CNN-based Gabor-type filters

A 2-D cellular neural network (CNN) circuit performing Gabor-type filtering as shown in Fig. 2 has been proposed by B. E. Shi [8]. Each pixel consists of two nodes corresponding to real and imaginary parts of the Gabor coefficient. The convolution kernel for pixel coordinate $\vec{r}$ is

$$h(\vec{r}) \propto e^{-\lambda|\vec{r}|}e^{j\vec{\omega_0}\vec{r}}, \tag{1}$$

where λ is the decay constant of the exponential envelop function, and $\vec{\omega_0} \equiv (\omega_{0x}, \omega_{0y})$ is a frequency vector with a specific direction. This direction is determined by the ratio of ω_{0y} to ω_{0x}; i.e., $\tan\theta = \omega_{0y}/\omega_{0x}$, where θ is the angle between the frequency vector and the x-axis. This is a unique and important feature of this circuit. Only by changing ω_{0y} and ω_{0x}, i.e., the conductances of the network, Gabor-type filtering with arbitrary frequencies and directions can be achieved in this circuit.

An example of numerical simulation results for impulse responses of the 2-D Gabor-type filter circuit is shown in Fig. 3. This result is nearly identical with the mathematical result obtained from Eq. 1.

B. PWM pixel unit circuit for pixel-parallel implementation of analog CNNs

In order to implement the analog CNN circuit as shown in Fig. 2, we have proposed a pixel unit circuit with arbitrary nonlinear functions based on pulse modulation techniques [4]. Our pixel unit circuit emulates the operation of the node in analog CNN circuits by discrete-time dynamics based on clock operation. A change in each node voltage is calculated using Kirchhoff's law, and the steady state is obtained by repeating the updating process. The dynamics of pixel node n implemented is

$$O_n(t+1) - O_n(t) = \nu[\sum_{j,k\in N_n} G_{jk}(O_j - O_k) + F_j(O_j - I_n)], \tag{2}$$

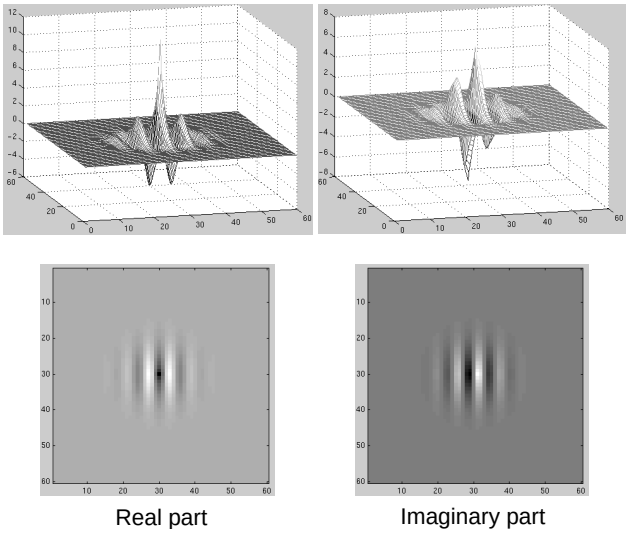


Figure 3: Impulse response of 2-D Gabor-type filter circuit (numerical simulation result).

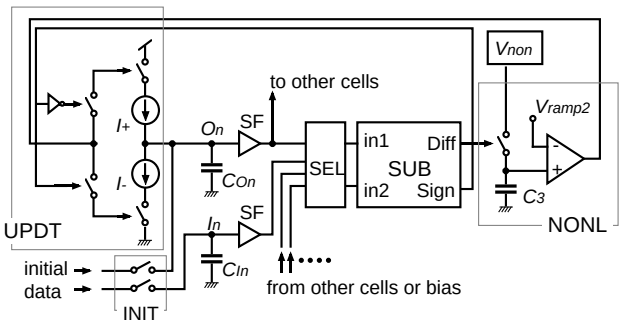


Figure 4: Pixel unit circuit using PWM signals. (SF is a source follower circuit used as an analog buffer, other circuit blocks are described in the text.)

where O_n and I_n are the node voltage and the input voltage, respectively; N_n represents neighbor nodes of n including node n itself; ν is a constant. Functions $G_{jk}(\cdot)$ and $F_j(\cdot)$ are arbitrary odd functions; although the Gabor-type filter circuit requires only linear functions, this pixel unit circuit can implement arbitrary odd functions as required for resistive-fuse networks.

Our pixel unit circuit is shown in Fig. 4. Voltages O_n and I_n are temporarily stored at capacitors C_{On} and C_{In}, respectively, and O_n is updated according to the discrete-time dynamics. The circuit shown in Fig. 4 is slightly different from the previously proposed one [4]. Since subtraction circuit *SUB* directly receives voltage inputs, the processing time can be shortened compared with the previous circuit. The detail of *SUB* is described in Ref. [6].

The updating process proceeds as follows:

1) Selector *SEL* selects a set of signals to be calculated, which corresponds to one term on the right side of Eq. 2.
2) Circuit *SUB* calculates the absolute value and the sign of the difference between the selected two signals. A pulse-width modulation (PWM) signal whose pulse width is proportional to the absolute value appears at node *Diff* and the sign bit appears at node *Sign*. The sign bit determines the updating direction of O_n.
3) The PWM pulse switches the voltage source V_{non} whose voltage waveform in the time domain is the same as the corresponding (nonlinear) function ($G_{jk}(\cdot)$ or $F_j(\cdot)$). Thus, capacitor C_3 holds the value of the corresponding term in Eq. 2.
4) The voltage stored in capacitor C_3 is again converted into a PWM pulse, and it switches the current source I_+ or I_-. Output O_n is thus updated by the corresponding term.
5) Repeating the above processes, O_n is updated by another term.

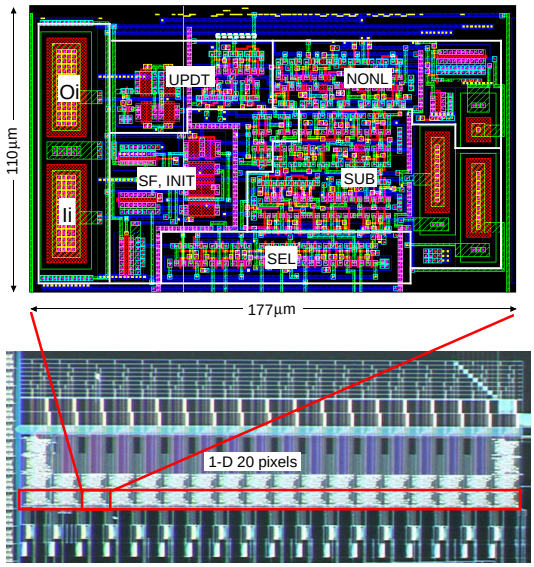


Figure 5: Pixel unit circuit layout and micro-photograph of a part of the PWM CNN test chip.

C. Design and measurement results of fabricated test chip

We designed a PWM pixel unit circuit using 0.6μm CMOS technology, and constructed a 1-D 20-pixel network. The layout image of the pixel unit circuit and a photograph of the fabricated chip are shown in Fig. 5. Each pixel has two unit circuits because the Gabor-type filter requires two nodes as described above. The supply voltage was 3.3 V, and the power consumption was 33 μW per pixel unit circuit.

This chip can also operate as a resistive-fuse network [6], here we show the measurement results for Gabor-type fil-

ter operation as shown in Fig. 6. This shows an impulse response for a period ($= 2\pi/\omega_0$) of 4 pixels, and the convergence time was about 600μs. The outputs were nearly identical with the numerical results. These results verifies our chip successfully operates as a Gabor-type filter.

IV. CONCLUSION

We proposed a feature extraction method consisting of coarse region segmentation by a resistive-fuse network and feature extraction by Gabor wavelet transforms. The pixel-parallel VLSI implementation based on the pulse modulation circuit architecture was described. We designed a pixel unit circuit and a test LSI chip with 1-D 20-pixels using 0.6 μm CMOS technology, and verified the basic operation by measuring the impulse response in the test LSI chip.

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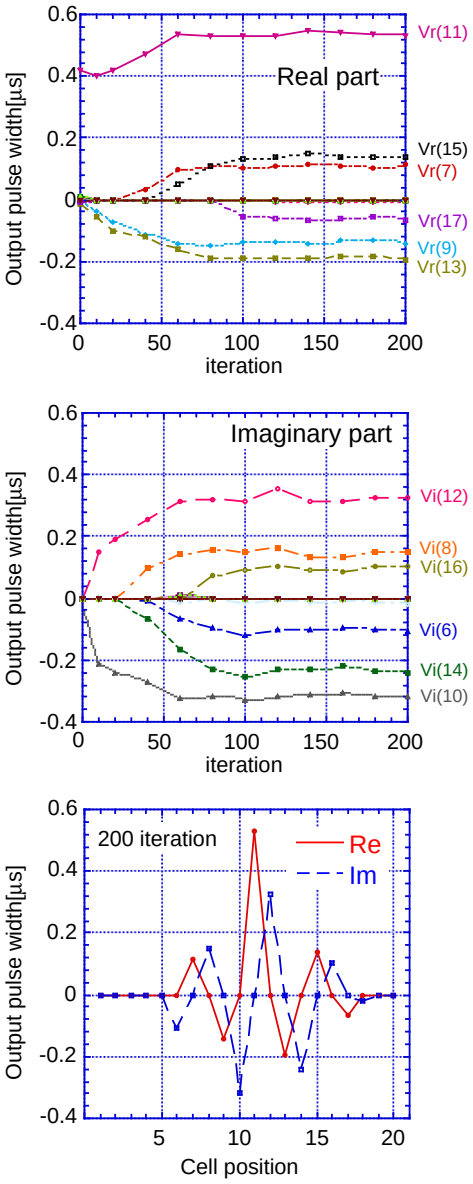

Figure 6: Measurement results of Gabor-type filer composed of the PWM pixel unit circuits: impulse response when the initial non-zero value is only given at pixel #11.