Nonlinear Dynamical Systems Utilizing Pulse Modulation Signals and a CMOS Chip Generating Arbitrary Chaos

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Abstract

This paper presents nonlinear dynamical systems utilizing pulse modulation signals suitable for VLSI implementation. The proposed circuits implement discrete-time continuous-state dynamics by analog processing in time domain. Arbitrary nonlinear transfer functions can be generated using the conversion from an analog voltage to a pulse-width modulation (PWM) signal. The nonlinear waveforms that have the same shape as the inverse function of the desired transfer function are supplied. A CMOS chip generating arbitrary chaos has been designed and fabricated using a 0.4μm CMOS process. Chaos using the tent map and logistic map has successfully been observed using the chip.

1. Introduction

Recent many studies have revealed the important role of nonlinear analog dynamics from the viewpoint of information processing. Chaotic neural networks[1] and nonlinear oscillator networks[2] are the typical examples. However, conventional VLSI neural hardware hardly implements such nonlinear dynamics.

Circuit architectures in conventional neural VLSI chips are usually classified into digital and analog. Digital approaches cannot implement analog dynamics essentially although they can have high precision and controllability. Analog approaches are obviously suitable for realizing analog dynamical systems, but the calculation precision is affected by various non-idealities in circuit components. Moreover, it is not easy in analog approaches to achieve arbitrary nonlinear, non-monotone transformation.

We have already proposed a new circuit technique generating arbitrary nonlinear functions by using conversion from an analog voltage to a pulse-width modulation (PWM) signal [3]. We have also proposed another circuit principle by using conversion from pulse-width/pulse-phase modulation (PWM/PPM) to analog voltage[4]. They make it possible to realize arbitrary discrete-time, continuous-state nonlinear dynamical systems. We designed an arbitrary chaos generator and a nonlinear oscillator and demonstrated their performance using HSPICE simulation [3-6].

In this paper, we present how to construct arbitrary nonlinear dynamical systems using PWM signals and describe detail design of an arbitrary chaos generator CMOS chip. It was fabricated using a 0.4μm CMOS process. The measurement results are shown and compared with the HSPICE simulation results.

2. PWM approach suitable for VLSI nonlinear dynamical systems

2.1. Features of PWM approach

From the viewpoint of information representation, the pulse-width modulation (PWM) method is one approach toward achieving time-domain information processing using pulse signals. Another approach is the pulse-density modulation (PDM) method, which has often been used for LSI implementation of neural networks [7-9].

The PWM approach implements continuous-state discrete-time dynamics, while the PDM approach can approximately implements continuous-state continuous-time dynamics. Discrete-time dynamics is not used in the real biological brains, but it has been thoroughly examined, and equivalent functions can be achieved in most cases. Moreover, *synchronous systems*, which obviously use discrete-time dynamics but do no necessarily mean *synchronous state updating*, have superior features in VLSI systems: high controllability and excellent matching with ordinary digital systems. They are also stable and robust against various disturbances arising in real VLSI systems. Thus, our PWM approach seems to be a suitable candidate for constructing large-scale *brain-like systems*.

From the viewpoint of VLSI circuit architecture, the PWM approach is realized in an analog-digital merged circuit architecture, where signals have dig-

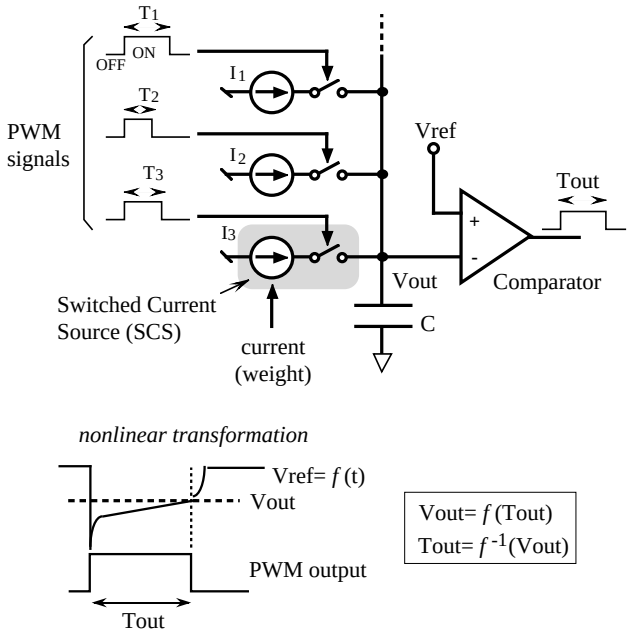

Figure 1. Weighted summation and nonlinear transformation using PWM signals

ital values in the voltage domain and analog values in the time domain. [10]. This PWM approach is suitable for large-scale integration of analog processing circuits because it matches the scaling trend in the Si CMOS technology and leads to low voltage operation; recently, the supply voltage in the most advanced VLSI chips is lowered around 1 V, thus the analog operation in the voltage domain becomes very difficult. It also achieves lower power consumption operation than traditional digital or PDM circuits because one data is represented by only one state transition in the PWM approach. This is another important superior point to the PDM approach in VLSI systems.

2.2. Arbitrary nonlinear dynamical systems constructed using an analog-digital merged circuit architecture

In general, an arbitrary nonlinear dynamical system represented by N variables, x_n, $(n = 1, 2, 3, \cdots, \mathrm{N})$, is defined by a set of iterated forms of arbitrary nonlinear transformations f_n:

$$x_n(t+1) = f_n(x_1(t), x_2(t), \cdots, x_N(t)),\ n = 1, 2, \cdots, N, \quad (1)$$

where discrete-time dynamics is assumed, When we consider systems for information processing, transformations f_n are not so complicated mathematically. The required operations to make f_n are multiplications and summations, or weighted summations, and nonlinear transformations with one variable.

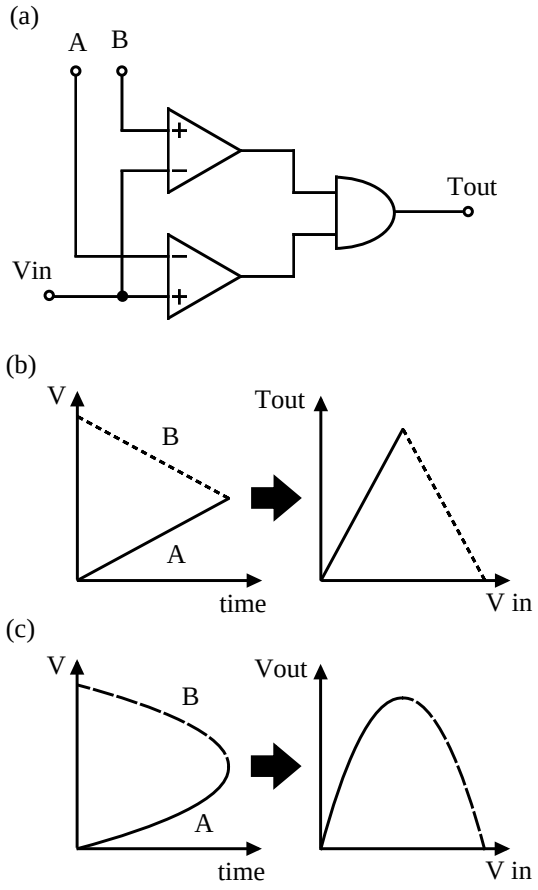

Figure 2. Arbitrary second-order nonlinear transfer function generator circuit using PWM signals

Our analog-digital merged circuit achieves weighted summations and nonlinear transformations with monotone functions such as sigmoidal functions as shown in Fig. 1.

PWM input signals having pulse-width T_i, $(i = 1, 2, 3, \cdots)$, drive the corresponding switched-current sources (SCS's), and currents I_i flow to capacitor C during period T_i. The number of charges stored in the capacitor, Q_{out}, and the terminal voltage of the capacitor, V_{out}, are

$$\begin{aligned} Q_{out} &= \sum_i I_i T_i, \quad (2) \\ V_{out} &= \frac{Q_{out}}{C} = \frac{\sum_i I_i T_i}{C}, \end{aligned}$$

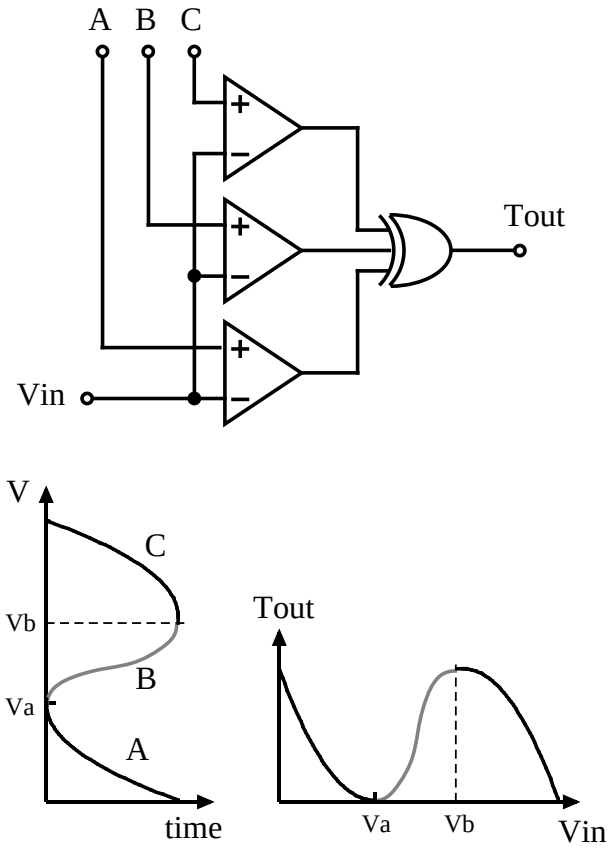

Figure 3. Arbitrary third-order nonlinear transfer function generator circuit

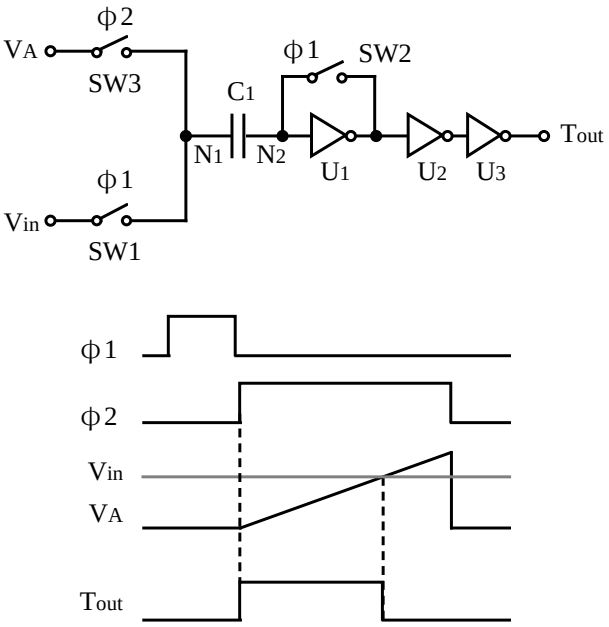

Figure 4. Clocked CMOS comparator circuit including S/H mechanism

respectively. Thus, the weighted summation of the PWM data is obtained in the form of the number of stored charges or the terminal voltage of a capacitor. A weight in summation is represented by a current value for each SCS.

The PWM output signal is made by comparing Q_{out} or V_{out} with a ramped reference value. A nonlinear transformation can be performed in this comparing process by preparing a nonlinear reference waveform. If the reference signal voltage V_{ref} nonlinearly varies in the time domain, i.e. $V_{ref} = f(t)$, where f is a nonlinear function, the pulse-width of output signal T_{out} expressed as a function of input voltage V_{out} is given by $T_{out} = f^{-1}(V_{out})$, where f^{-1} is the inverse function of f. The function f is, however, limited to a monotone function in this scheme.

Non-monotone functions can be generated by combining the outputs of plural comparators. Figure 2 and 3 show examples of making second-order and third-order nonlinear functions, respectively [3].

The reason why this approach is useful is that we can easily generate arbitrary nonlinear functions as a function of time by using various relaxation oscillator circuits or D-A converters, while it is very difficult to generate arbitrary nonlinear transfer functions in voltage or current domains.

Since the PWM-charges-PWM transformations are analog operations, much attention should be paid in designing the corresponding circuits. However, establishing the design criteria is easier than in the pure analog approach because analog parts in PWM circuits are localized.

3. Circuit design

We use a clocked CMOS comparator consisting of CMOS inverters and a capacitor as shown in Fig. 4. This comparator has a simpler configuration, consumes less power, and is more suitable for low-voltage operation than comparators using a differential-pair. Clocked operation is suitable for making PWM signals because it is a discrete-time operation.

This comparator consists of inverters U_1 to U_3, a capacitor C_1, and switches SW_1 to SW_3 controlled by

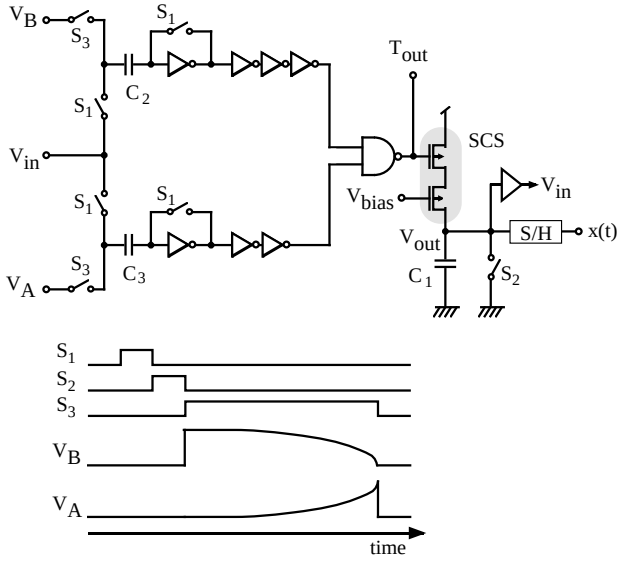

Figure 5. Arbitrary chaos generator circuit with second-order nonlinearity designed using clocked CMOS comparators

clocks ϕ_1 and ϕ_2. Capacitor C_1 holds the difference between the input voltage V_{in} and the threshold voltage of inverter U_1, V_{th}, during the ϕ_1 period. This operation compensates for fluctuation of the threshold voltage in inverter U_1. In the ϕ_2 period, a monotonically ramped reference voltage V_A is supplied to the capacitor node N_1. When V_A reaches the V_{in}, the voltage of the other capacitor node (the input node of inverter U_1), N_2, reaches V_{th} and the inverter is inverted. Thus, an output pulse having a width T_{out} is generated. In this comparator operation, the capacitor C_1 and the switch SW_1 operate as a sampling and holding (S/H) circuit.

Thanks to the S/H mechanism of the clocked CMOS comparator, iterated operation can be achieved using a simple circuit configuration. As a simple example of nonlinear dynamical systems, Fig. 5 shows an arbitrary chaos generator with second-order nonlinearity.

In this circuit, the scheme shown in Fig. 2 is used for generating second-order nonlinearity. By the S_1 signal, the terminal voltage of capacitor C_1, V_{out}, is held as the state value $x(t)$, and at the same time, it is transferred to the nodes of capacitor C_2 and C_3 in the clocked comparators through a buffer. Then, V_{out} is reset by the S_2 signal. Next, by the S_3 signal, the PWM output, T_{out}, drives the SCS, and voltage V_{out} is updated. Thus, this circuit implement the following

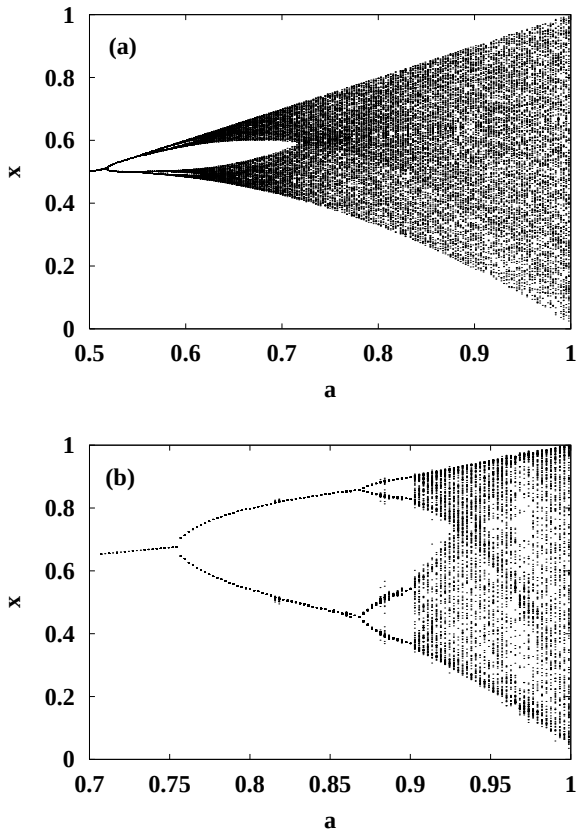

Figure 6. Bifurcation diagrams obtained by HSPICE simulation: (a) tent map and (b) logistic map

dynamics:

$$\begin{aligned} x(t+1) &= f(x(t)), \\ T_{out}(t+1) &= f(T_{out}(t)), \end{aligned} \tag{3}$$

where f is a second-order nonlinear function defined by the voltage waveforms supplied at node A and B. It is noted that we can simultaneously obtain both voltage and PWM signals following the given dynamics. This is a unique feature of our analog-digital merged architecture.

4. SPICE simulation results

Two examples of generating chaos are given by tent and logistic maps. A tent map is

$$x(t+1) = \begin{cases} 2ax(t) & \text{for } x(t) < 1/2, \\ 2a(1-x(t)) & \text{for } x(t) \geq 1/2, \end{cases} \tag{4}$$

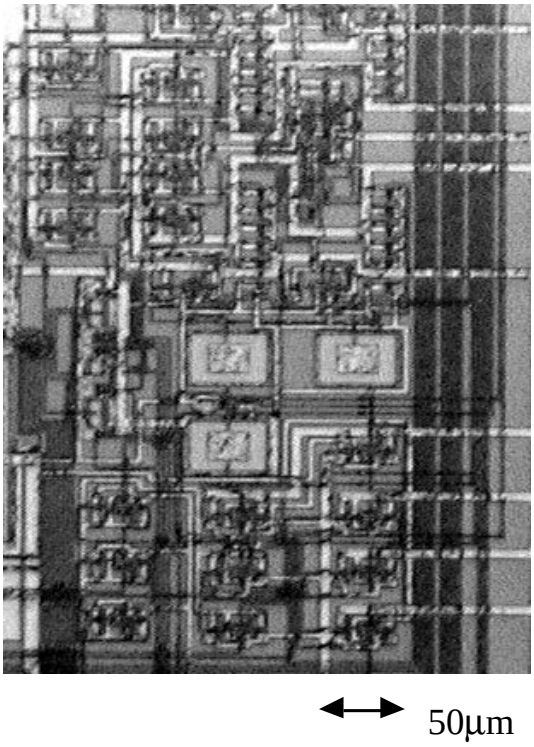

Figure 7. Micro-photograph of the arbitrary chaos generator circuit (without a buffer)

where a is a parameter ranging from 0 to 1. The behavior of $x(t)$ is chaotic when $a > 0.5$. A logistic map is

$$x(t+1) = 4ax(t)(1 - x(t)). \quad (5)$$

The behavior of $x(t)$ is chaotic when $a > 0.89$.

We performed circuit simulations (HSPICE) of our circuit and obtained bifurcation diagrams as shown in Fig. 6. The device parameters used were based on a 0.4 μm CMOS process, the supply voltage was 3.3 V, and the clock period was 800 nsec. The parameter a was modified by changing V_{bias}.

In Fig. 6(b), the diagram is blurred at $a \approx 0.82$ and $a \approx 0.88$. This is because one attractor point is $x = 0.5$ in these cases. It is difficult to achieve highly accurate transformation at the top of the parabola because in the given waveforms V_A and V_B, dV/dt is diverged as can be seen in Fig. 5.

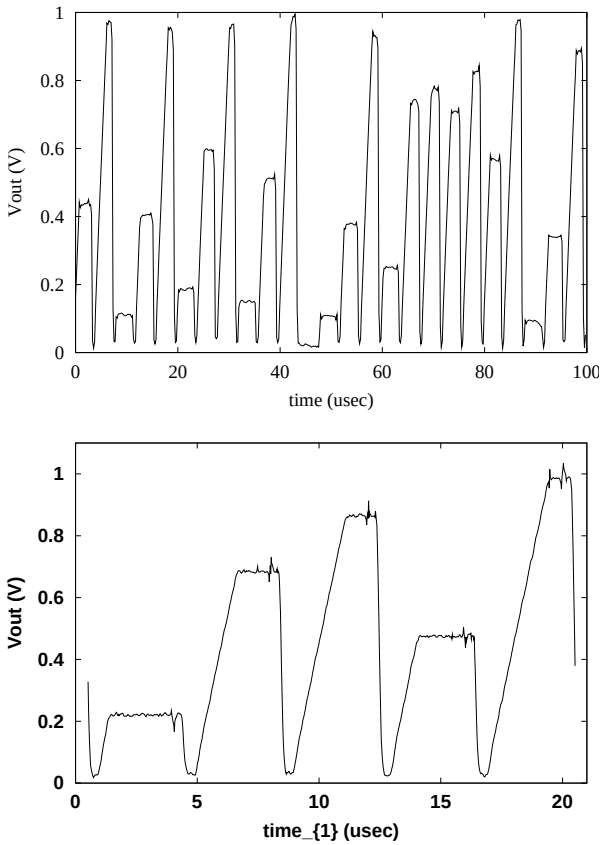

Figure 8. Chaotic waveforms observed in the logistic map using CMOS chaos chip. The starting time (t=0) is arbitrary.

5. A CMOS chip generating arbitrary chaos and its measurement results

We fabricated an arbitrary chaos generator chip using a 0.4μm CMOS process as a proof-of-concept. The circuit is based on Fig. 5. The capacitances are $C_1 = 5$ pF, $C_2 = C_3 = 1$ pF. As a buffer, both a voltage follower of an on-chip opamp and a CMOS source follower were used. The former gives high accuracy but occupies the large chip area. The latter makes whole circuit compact but the input-output characteristic is not completely linear. However, this nonlinearity can be compensated for by modifying the reference waveforms. For simplicity, the following are the results obtained using the voltage follower. A micro-photograph of the arbitrary chaos generator circuit without the buffer part is shown in Fig. 7.

In the following measurement, the reference volt-

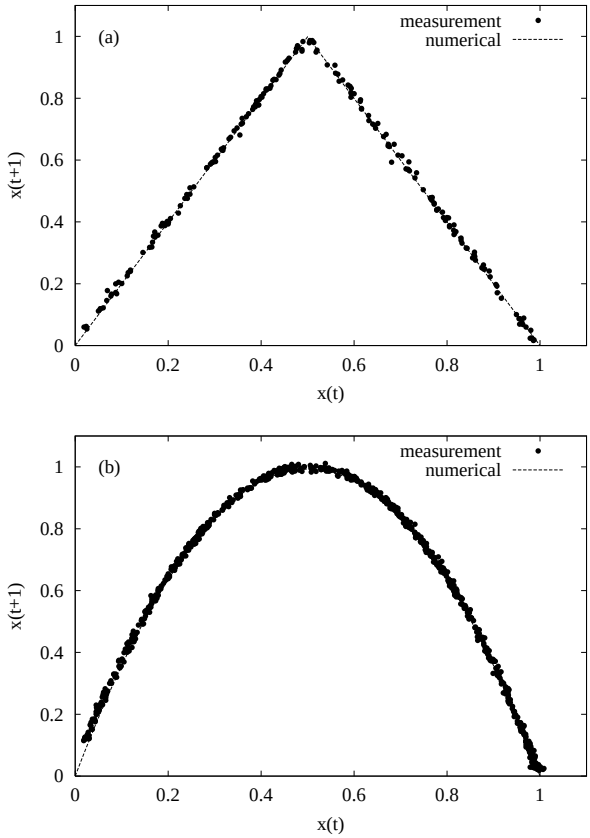

Figure 9. Return maps obtained by observed waveforms. (a) tent map, (b) logistic map.

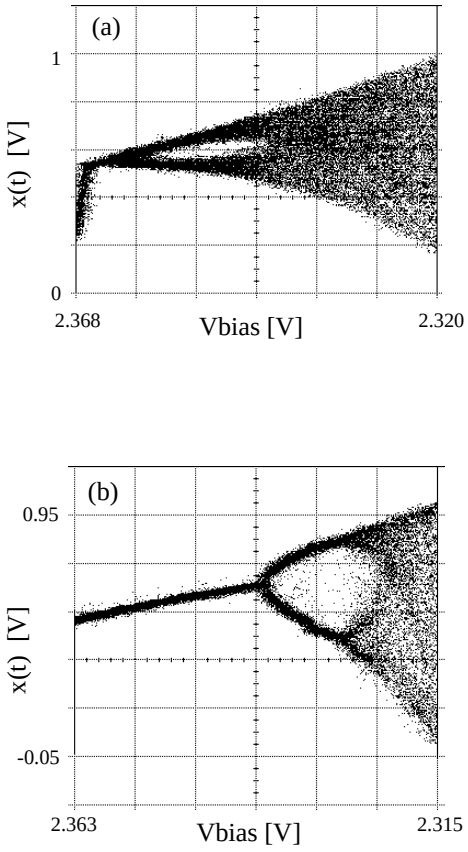

Figure 10. Bifurcation diagrams observed on the oscilloscope screen. (a) tent map, (b) logistic map.

age waveforms V_A and V_B were given by the external arbitrary waveform generator equipment.

Chaotic waveforms were obtained by observing the time series of V_{out} as shown in Fig. 8, where the nonlinear transformation was a logistic map, and the clock period was 4 μsec. The disturbances observed at the plateau regions are attributed to the S_1 control signal.

Figure 9 shows return maps in a tent map and a logistic map obtained by the observed waveforms, where $a \approx 1$. The sampling timing is just before the disturbance by the S_1 clock. Both results demonstrate high accuracy of the chaos generator chip.

Figure 10 shows bifurcation diagrams observed on the oscilloscope screen. In order to observe the bifurcation diagram on the screen, V_{bias} was ramped linearly with around 20 Hz. The oscilloscope is set at the X-Y and *point* plot mode.

The observed bifurcation diagrams are similar to the HSPICE simulation results shown in Fig. 6. The relatively large noise is partially due to sampling timing of the oscilloscope, and partially due to disturbance by the S_1 clock.

6. Conclusion

We presented nonlinear dynamical systems that can be constructed based on our analog-digital merged architecture. In our architecture, conversion from PWM to analog voltage or from analog to PWM is effectively used for weighted summation or nonlinear transformation. The nonlinear transformation described in this paper is arbitrary and analog. This cannot be realized in the ordinary analog approach, nor can the digital approach such as using look-up-tables.

We fabricated an arbitrary chaos generator CMOS chip using a 0.4μm CMOS process. The measurement results demonstrated that the calculation precision of the chip is high enough to generate chaos. The future

work is chaos generation in dynamics with more than one variable and/or more than second-order nonlinearity.

ACKNOWLEDGMENT

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