A Multi-Nano-Dot Circuit and Structure Using Thermal-Noise Assisted Tunneling for Stochastic Associative Processing

Takashi Morie*, Tomohiro Matsuura, Makoto Nagata, and Atsushi Iwata

Graduate School of Advanced Sciences of Matter, Hiroshima University,
Higashi-Hiroshima, 739-8526 Japan.
Phone: +81-824-24-7686, Fax: +81-824-22-7195, E-mail: morie@dsl.hiroshima-u.ac.jp

Abstract – The single-electron circuit and nanostructure described in this paper are designed for stochastic associative processing, which is an expanded version of ordinary associative memory processing. In stochastic associative processing, the association probability of each stored pattern depends on the similarity between the stored pattern and the input pattern. Such unique processing is useful for sequential stochastic association and for clustering for vector quantization. Conventional single-electron circuits operate only at very low temperature for practical junction capacitance; i.e., 30 K for 0.1 aF, because the charging energy in these circuits is directly related to the tunnel junction capacitance. Our multi-nano-dot circuit and structure operate at room temperature with a junction capacitance around 0.1 aF by using tunneling processes assisted by thermal noise. We analyze the operation of this circuit in detail and propose for it a stochastic associative processing operation, where the detection timing of the electron position controls the association probability distribution.

–Keywords–

single-electron circuit, nanostructure, nano-dot array, stochastic associative processing, thermal-noise assisted tunneling, stochastic resonance

1 Introduction

Single-electron circuits composed of nanostructures are promising in the construction of ultimately high-density VLSI systems after the era of CMOS technology. However, from the viewpoint of system applications, they have intrinsic difficulties: slow operating speed and insufficient reliability [1] due to stochastic tunneling events and serious background charge sensitivity [2]. Therefore, multi-stage logic architectures used in conventional digital circuits are not suitable for constructing single-electron VLSI circuits. The development of CMOS VLSI technology will probably continue for another decade or two, thus new architectures should be developed to allow single-electron circuits to coexist with CMOS circuits. At the same time, new single-electron circuits based on new information processing principles should also be invented. Our strategy to achieve single-electron VLSI circuits is summarized in Fig. 1 [3].

Examples of such circuits include those we have already proposed using single-electron transistors [3] and those using the Coulomb repulsion effect between nano-dots [4]. These circuits measure the Hamming distance, which is the number of unmatched bits between two digital data, and are core circuits for intelligent information processing such as associative memories and pattern recognition. However, these circuits have an intrinsic drawback: for practical junction capacitance they can be operated only at very low temperatures; e.g., 30 K for 0.1 aF. This is because the charging energy in these circuits is directly related to the tunnel junction capacitance. Conversely, very low capacitance, such as 0.01 aF, is required for room-temperature operation. This capacitance value, corresponding to that between quantum dots with a diameter of around 0.1 nm, is very difficult to realize.

To overcome this problem, we recently proposed another circuit, composed of multi-nano-dots, that operates at room temperature with a practical junction capacitance around 0.1 aF by using tunneling processes assisted by thermal noise [5].

In this paper, we analyze the operation of this circuit in detail and propose for it a stochastic associative processing operation, where the detection timing of the electron position controls the association probability distribution.

2 Stochastic Associative Processing

Ordinary associative processors compare the input pattern with all of the stored patterns, and deterministically extract the stored pattern most similar to the input. In contrast, the stochastic associative processor does not always extract the most similar pattern. Instead, the second or third most similar pattern is sometimes extracted with an association probability, depending on the similarity of the pattern to the input [6]. This concept offers an approach to intelligent information processing that differs from the conventional deterministic approach. Useful and unique examples of this new type of processing are sequential stochastic association [7] and clustering for vector quantizer [8].

The sequential association can be achieved by feeding back the associated output to the input. Repeating the association, the stochastic associative processor sequentially outputs various patterns similar to the immediately preceding one. The average association range can be changed by changing the association probability distribution as a function of similarity. It is difficult for conventional deterministic associative processors to generate such a human-like association sequence.

Vector quantization is a technique to represent many input data vectors by comparatively few reference vectors in a multi-dimensional space. The best reference vector set is that which has the minimum distortion error between data vectors belonging to each cluster and that cluster's representative reference vector. Various clustering algorithms to obtain better reference vectors from incoming sample data have been reported so far [9-11].

The clustering algorithm using stochastic association is very simple. A reference vector is selected stochastically based on the evaluation of the distance between the input data vector and each reference vector. Then, the selected reference vector is slightly updated in order to approach to the input data vector. When we repeat these processes, most reference vectors converge to the points representing the data clusters. We have confirmed through several examples that our new clustering algorithm is most efficient compared with the conventional clustering algorithms [8]. In this algorithm, changing the association probability distribution during repeated updating processes is essential for obtaining better reference vectors. It is noted that the clustering algorithms require analog data processing. In the following, we will use digital data, but we discuss in Sec. 6 how analog data can be treated in the same architecture.

3 Stochastic Associative Processor Architecture Using Nanostructures

Here, we treat patterns represented by a set of binary data; such a set is also referred to as a word. The associative processors compare each input pattern bit with the corresponding stored pattern bit by exclusive-NOR logic operation, and the matching results are represented by a Hamming distance. As a result, the associative processor deterministically extracts the stored pattern having the shortest Hamming distance.

Stochastic associative processing can be achieved by a bit-comparison operation with random fluctuation based on quantum mechanical behaviors of electrons in nanostructures. Figure 2 shows the architecture of a stochastic associative processor that uses nanostructures. Each word-comparator (WC) consists of N bit-comparators (BCs) and evaluates the similarity between an input pattern and each stored pattern. The BCs consist of nanostructures and perform bit-comparison with random fluctuation. Thus, the input pattern is *stochastically* compared with the stored patterns by WCs. The result of a WC's comparison is expressed as the total number of electrons released from the BCs. The electrons are collected at each capacitor. The results of all of the WCs are fed into a Winner-Take-All (WTA) circuit, which deterministically extracts the stored pattern evaluated as that most similar to the input. The WTA circuit can be constructed by CMOS devices.

4 A Multi-Nano-Dot Word-Comparator Circuit and Structure Using Thermal-Noise Assisted Tunneling

4.1 Circuit and structure

Let us assume nano-dot structures constructed on a MOS transistor gate electrode as shown in Fig. 3. Each nano-dot structure consists of a pair of one-dimensional (1D) dot arrays: A_v (D_{v1}, D_{v2}, D_{v3}) and A_h ($D_1, \cdots, D_n, D_c, D_n, \cdots, D_1$), where n is the number of dots at a side of A_h. The array A_h has dot D_e outside of each end. The capacitance C_o corresponds

to the gate capacitance of an ultrasmall MOS transistor. A bit (1 or 0) of the input and stored data is represented by whether or not an electron is placed at each end dot D_e. (Alternatively, an appropriate voltage corresponding to a bit may be applied directly at D_e). Bias voltages are applied to the plate P_c over D_c (V_{pc}), to the nodes outside of D_e (V_e), and to the backgate of the MOS transistor (V_{bg}).

An electron e_M is introduced at the center dot D_c of the 1D array A_h. This can be achieved by using Fowler-Nordheim tunneling from, for example, the electrode P_c. Electron e_M can move along array A_h through tunneling junctions C_j, but it cannot move to either of D_e's or to D_{v3} through normal capacitor C_2. Each dot structure works as an exclusive-NOR logic gate (bit comparator) with random fluctuation, as explained below.

4.2 Stabilization process

By applying appropriate bias voltages V_{pc}, V_e, and V_{bg}, the profile of the total energy as a function of the position of e_M along the 1D array A_h has a minimal value at D_c, as shown in Fig. 4. For *1-1 state*, where electrons are placed at both D_e's, the energy at D_1 rises, and thus e_M is most strongly stabilized at the center position. Therefore, the difference between *0-0 state* and *1-0 (or 0-1) state* is important for correct bit-comparator operation. In the two states, the energy profile has another minimal value at D_1. The energy barrier height for e_M located at D_c is approximately determined by the total capacitance for e_M and bias voltages. The greater number of serial capacitance connections causes higher energy barriers, and the energy differences can be much larger than the thermal energy at room temperature even if the tunneling junction capacitance C_j is around 0.1 aF.

The energy barrier at the "0" side in *1-0 (0-1) state* becomes lower than that in *0-0 state* because of the Coulomb repulsion force of the electron placed at the opposite D_e, as shown in Fig. 4. Thus, e_M in *1-0 (0-1) state* can more easily overcome the barrier when assisted by thermal noise at non-zero temperature and it then moves to D_1 at the "0" side. As a result, there exists a certain time span t_0 within which e_M in *1-0 (0-1) state* moves to D_1 while e_M in *0-0 state* stays at D_c.

4.3 Detection Process

After spending t_0, the vertical dot array A_v detects whether or not e_M stays at D_c, by changing the bias voltages if necessary. Only if e_M stays at D_c, array A_v is polarized and an electron is induced at the gate electrode of C_o. (In order to achieve stable polarization, at least three dots are required in A_v). The total number of electrons induced at the gate electrode is proportional to the number of matched bits; this reflects the gate voltage V_o, and it can be measured by the source-drain current of the MOS transistor. Thus, the Hamming distance can be measured by this MOS transistor with nanostructure arrays.

If this detection process starts just after t_0, the most accurate bit comparison operation is achieved, although some statistical fluctuation remains. However, if the detection timing (t_d) is shifted from t_0, an arbitrary amount of fluctuation can be introduced in the bit comparison result. Thus, controlled stochastic association can be achieved, which is necessary in order to apply the stochastic association model to various types of intelligent information processing effectively.

5 Simulation Results

We analyzed the proposed circuit shown in Fig. 3 by using a Monte Carlo single-electron simulator [3], where the tunnel junction capacitance C_j is 0.1 aF and tunnel resistance R_t is 5 MΩ, and other parameters are shown in Fig. 3. In this case, the dot diameter is assumed to be around 1 nm. The bias voltages applied were $V_{pc} = 0$ V, $V_e = 1.15$ V, $V_{bg} = 0$ V for the e_M stabilization process, and $V_{pc} = 0$ V, $V_e = 1.8$ V, $V_{bg} = 3$ V for the e_M position detection process.

Figure 5 shows the total energy profiles at the "0" state side of A_h as a function of the position of e_M and as a parameter of n, where the energy when e_M is located at D_c is defined as zero. The time dependence of the position of e_M for $n = 2$ and 4 is also shown. It is confirmed from these results that (1) when $n = 2$, no barrier is formed and the position of e_M fluctuates due to thermal noise (the case of $n = 3$ also has the same results); (2) when $n \geq 4$, the barrier height for e_M at D_c is larger than the thermal energy at room temperature (i.e. 26 meV), and the barrier height in *1-0 (0-1) state* is lower than that in *0-0 state*.

Figure 6 shows the relationship between operating temperature and time (t_M) required until e_M moves to

D_1. The closed and open circles indicate t_M in many trials at *1-0 state* and *0-0 state*, respectively. Because the moving process assisted by thermal noise is purely stochastic, t_M scatters over a wide range. However, time span t_0, defined in the previous section, can be determined from these simulation results.

In order to determine t_0 precisely, we measured t_M for 100 simulations for *1-0* and *0-0 states* with different seeds for random number generation. The 100 data obtained for t_M were sorted in increasing order and numbered from 1 to 100. The assigned number means the number of electrons that move to D_1 within the corresponding t_M. Therefore, the relationship between t_M and the assigned number can approximately be considered as the probability that e_M moves to D_1 as a function of time. The results obtained at room temperature (300 K) are shown in Fig. 7. The optimum t_0 is obtained as the time having the smallest overlap between the two states; it is about 1 μs. It should be noted here that t_0 depends on tunneling resistance R_t. If lower tunneling resistance is available, t_0 becomes shorter.

From Fig. 7, we can obtain the probability of wrong detection, that is, the conditional probability that a given *1-0 state* is detected as *0-0 state* or vice versa. For example, when the detection timing is 10^{-7} sec, the probability that e_M moves to D_1 at *1-0 state* is only 20%. This means that wrong detection occurs with a probability of 80%.

By using this effect, we can add fluctuation to the bit comparison operation. However, in the above case, it must be noted that fluctuation can be added only in *1-0 state*. Bit-matched (*1-1* and *0-0*) states always answer correctly. Therefore, a comparison between patterns with a shorter Hamming distance is performed more deterministically. This means that a stochastic association operation cannot be achieved. An easy way to overcome this difficulty is to reverse the input bit pattern. Although this leads to a deterministic comparison between patterns with a longer Hamming distance, but such patterns are seldom associated, and thus it hardly affects the stochastic association operation.

Figure 8(a)-(c) show association probability distributions as a function of the Hamming distance for some t_d. In these simulations, the input pattern was (1,1,1,1), and the stored reference patterns were (1,1,1,1), (1,1,1,0), (1,1,0,0), (1,0,0,0), and (0,0,0,0). These reference patterns were reversed when they were applied to the multi-nano-dot circuit, for the reason described above. With the number of electrons indicating the results of Hamming distance evaluation with fluctuation, the reference pattern having the smallest evaluation result became the winner. If two or more reference patterns had the same number of electrons, we determined the winner stochastically. The simulations were repeated 100 times with different seeds for random number generation. The number of trials when a given reference pattern becomes a winner is approximately proportional to the probability that it is associated. The simulation results shown in Fig. 8 confirm that, as t_d becomes further apart from t_0 ($= 1$ μs in this case), the association probability distribution becomes flatter. Thus, the association probability distribution is controlled by changing t_d.

Figure 9 shows the time dependence of voltage V_o as a parameter of the Hamming distance for a 4-bit word comparator at room temperature, where the voltage for a distance of 0 bits is defined as 0 V. The voltage changes are proportional to the Hamming distance, and the voltage difference per bit is larger than 1 mV, which is large enough to detect with a CMOS circuit.

6 Discussion

Our bit-comparator circuit composed of nano-dot arrays works only at non-zero temperatures because at 0 K, e_M can never escape from D_c, the valley of the energy profile. Furthermore, the time span t_0 depends on the operating temperature. Conversely, for a given t_0, an appropriate amount of thermal noise is required; if the thermal noise is too small, electron e_M in *1-0 (0-1) state* cannot escape from D_c, thus no bit comparison is achieved. On the other hand, if thermal noise is too large, e_M in both *0-0 state* and *1-0 (0-1) state* escapes from D_c, and thus the two states cannot be distinguished. In this sense, it can be considered that this circuit utilizes a *stochastic resonance effect* [12] by thermal noise.

Additional charge effects due to offset, parasitic and/or surplus charges and the effect of device parameter fluctuation effect are important issues to be considered. The addition of charges comparable to the elementary charge causes a fatal error in bit comparison operation. However, introducing only one electron to the multi-nano-dot array does not seem to

be difficult, judging from the experimental results for nanocrystalline floating-dot MOSFET devices [13]. Furthermore, if plural nano-dot arrays are used for one bit comparison, the probability of such an error occurring can be reduced due to the averaging effect, which is indicated in our strategy shown in Fig. 1. Thus, a circuit based on the proposed structure will operate successfully even if the fabrication technology is not yet fully mature.

Although the above sections assume the use of digital data, analog data can be treated in the same circuit by using pulse-width modulation (PWM) signals, which have a digital amplitude and an analog pulse width [14]. Instead of a Hamming distance, a Manhattan distance, the summation of the absolute value of difference, is evaluated by using this nanostructure. The clustering algorithm using stochastic association for vector quantization mentioned in Sec. 2 can use this distance evaluation approach.

The proposed nanostructure has not yet been fabricated using the present VLSI technology. However, the basic technology of nanocrystalline floating-dot MOSFET devices, which are closely related to our structure, is now being developed [13, 15, 16]. Fabrication technology of self-organized nanostructures using gold particles is also being developed [17]. Furthermore, well-controlled self-assembly processes using molecular manipulation technology, especially that using DNA [18], would be utilized to fabricate our nanostructure. Thus, our nanostructure could be constructed in the near future.

7 Conclusions

A new operating principle of a multi-nano-dot circuit using thermal noise was proposed. This circuit can operate at room temperature, and the operating speed is determined by the tunneling resistance and operating temperature. The circuit can also implement controllable stochastic associative processing by using bit-comparison operation with random fluctuation.

Effective utilization of noise will be a key to creating new intelligent information processing algorithms and nano-scale functional devices. The circuit and structure described here comprise a promising example for such an approach.

Acknowledgments

The authors wish to thank Prof. Masataka Hirose for his support. This work has been supported by the Core Research for Evolutional Science and Technology (CREST) from Japan Science and Technology Corporation (JST).

References

[1] S. Shimano, K. Masu, and K. Tsubouchi, *Jpn. J. Appl. Phys.*, **38**, 403 (1999).

[2] R. H. Chen, A. N. Korotkov, and K. K. Likharev, *Appl. Phys. Lett.*, **68**, 1954 (1996).

[3] T. Yamanaka, T. Morie, M. Nagata, and A. Iwata, *Nanotechnology*, **11**, 154 (2000).

[4] T. Morie, T. Matsuura, S. Miyata, T. Yamanaka, M. Nagata, and A. Iwata, *Superlattices & Microstructures*, **27**, 613 (2000).

[5] T. Matsuura, T. Morie, M. Nagata, and A. Iwata, in *Ext. Abs. of Int. Conf. on Solid State Devices and Materials*, Sendai, Japan (2000), p. 306.

[6] M. Saen, T. Morie, M. Nagata, and A. Iwata, *IEICE Trans. Electron.*, **E81-C**, 30 (1998).

[7] T. Yamanaka, T. Morie, M. Nagata, and A. Iwata, *IEICE Trans. Electronics*, **E84-C**, 1723 (2001).

[8] T. Morie, T. Matsuura, M. Nagata, and A. Iwata, in *Advances in Neural Information Processing Systems 14*, edited by T. G. Dietterich, S. Becker and Z. Ghahramani, MIT Press, (2002), to appear.

[9] K. Rose, E. Gurewitz, and G. C. Fox, *Physical Review Letters*, **65**, 945 (1990).

[10] T. Kohonen, *Self-Organization and Associative Memory*, Springer-Verlag, Berlin (1984).

[11] T. M. Martinetz, S. G. Berkovich, and K. J. Schulten, *IEEE Trans. Neural Networks*, **4**, 558 (1993).

[12] A. R. Bulsura and L. Gammaitoni, *Physics Today*, **49**, 39 (1996).

[13] A. Kohno, H. Murakami, M. Ikeda, S. Miyazaki, and M. Hirose, *Jpn. J. Appl. Phys.*, **40**, L721 (2001).

[14] A. Iwata and M. Nagata, *IEICE Trans. Fundamentals.*, **E79-A**, 145 (1996).

[15] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbé, and K. Chan, *Appl. Phys. Lett.*, **68**, 1377 (1996).

[16] R. Ohba, N. Sugiyama, J. Koga, K. Uchida, and A. Toriumi, in *Ext. Abs. of Int. Conf. on Solid State Devices and Materials*, Sendai, Japan (2000), p. 122.

[17] S. Huang, G. Tsutsui, H. Sakaue, S. Shingubara, and T. Takahagi, *J. Vac. Sci. Technol. B*, **18**, 2653 (2000).

[18] R. A. Kiehl, in *Extended Abstracts, 4th International Workshop on Quantum Functional Devices (QFD2000)*, Kanazawa, Japan (2000), p. 49.

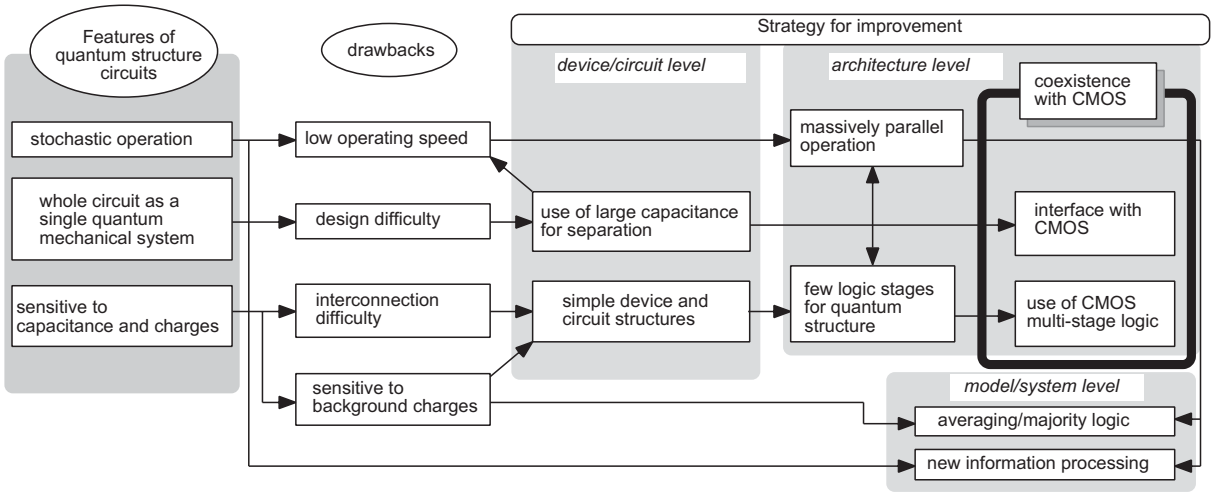

Figure 1: Our strategy to achieve nanostructure VLSI circuits.

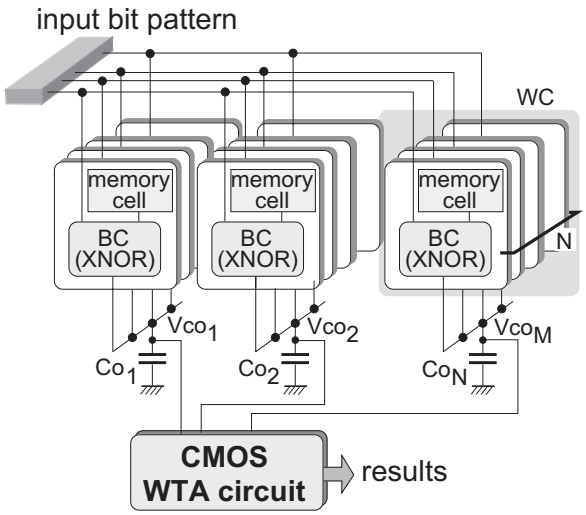

Figure 2: Architecture of the stochastic associative processor.

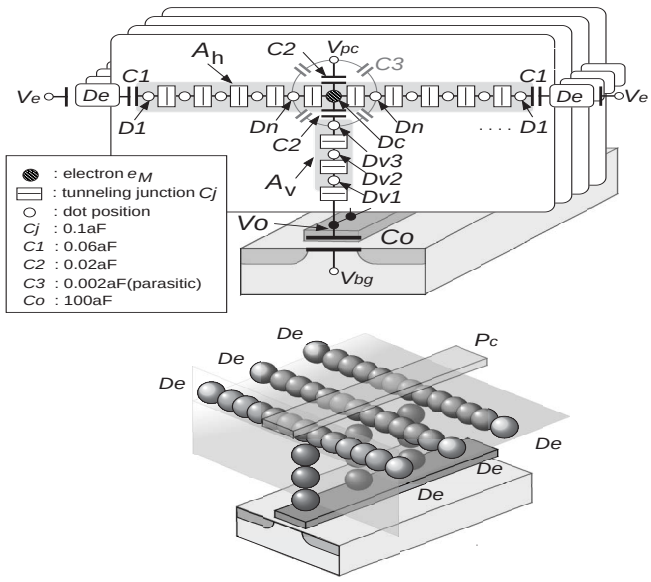

Figure 3: Multi-nano-dot circuit and image of a structure.

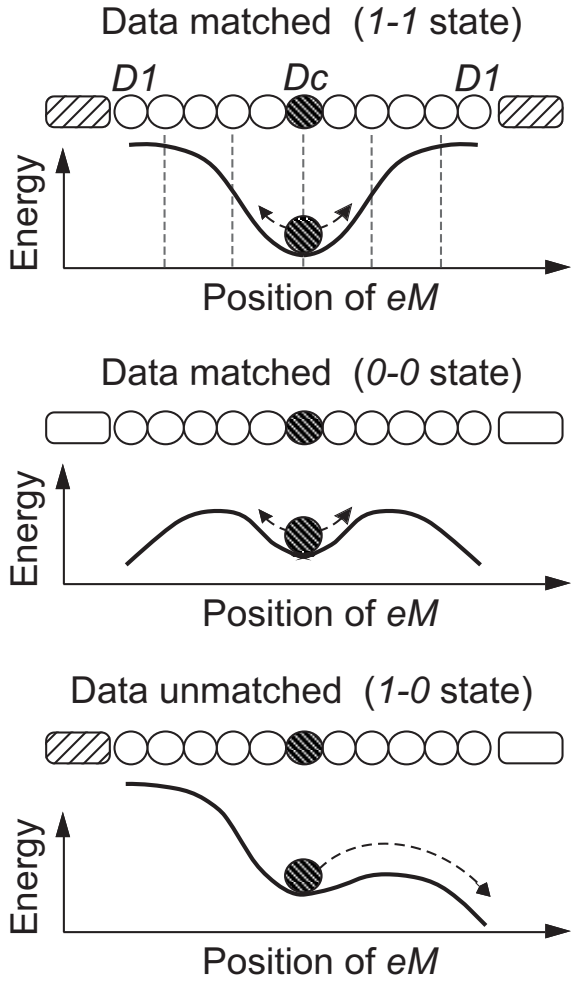

Figure 4: Schematics of total energy profile of 1D dot-array structure.

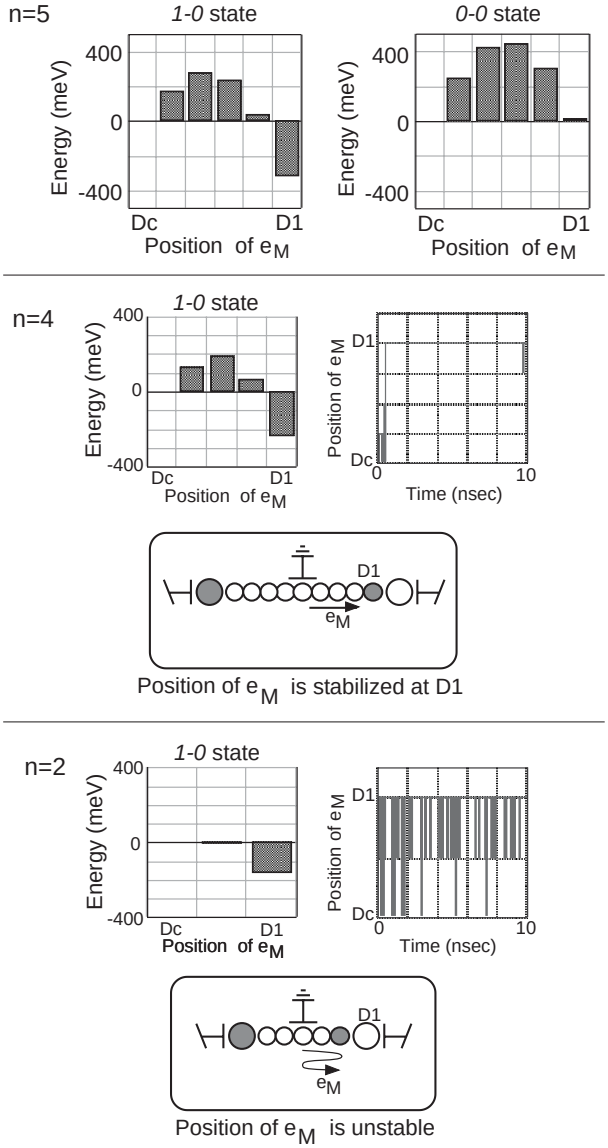

Figure 5: Energy profiles for electron e_M at the "0" state side in 1D dot array structures. The dependence of dot number n on barrier height can be seen. For $n = 2$ and 4, the time dependence of the position of e_M is also shown.

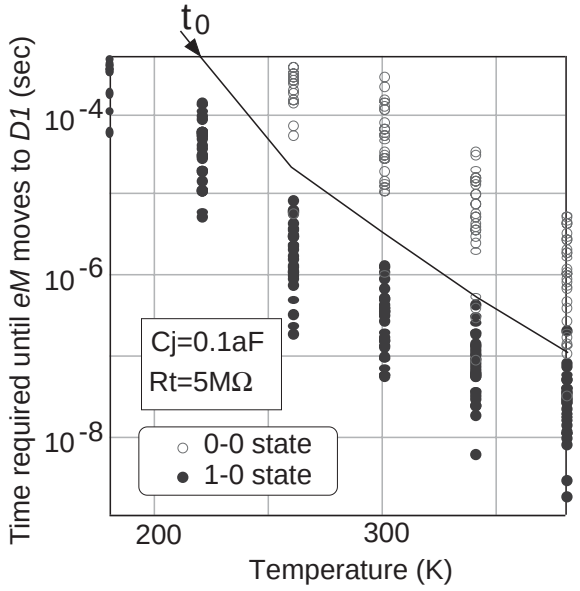

Figure 6: Relation between operating temperature and time when e_M moves to D_1.

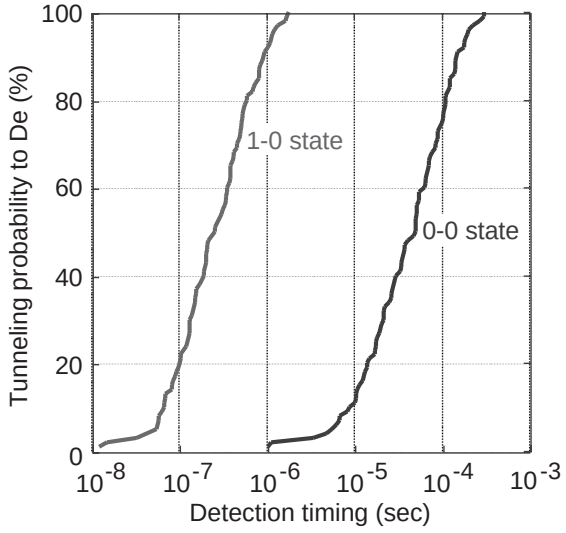

Figure 7: Probability that e_M moves to D_1 as a function of detection timing.

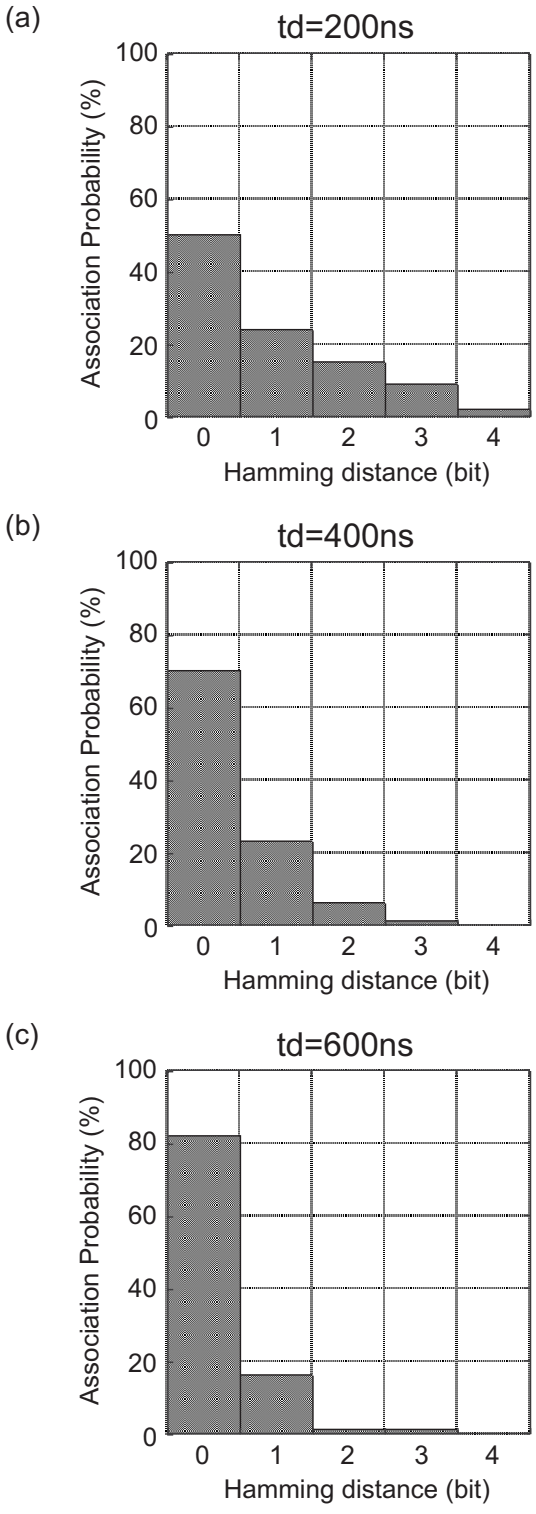

Figure 8: Association probability distribution as a function of Hamming distance for various detection timing t_d.

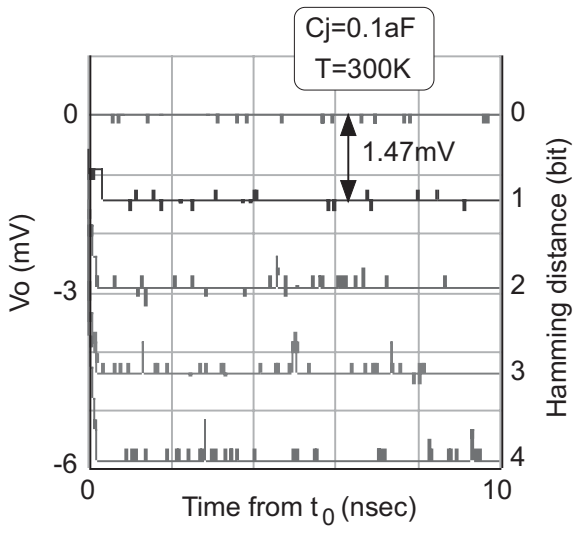

Figure 9: Time dependence of voltage V_o as a parameter of the Hamming distance.