Nonlinear Function Generators and Chaotic Signal Generators Based on Pulse-Phase Modulation

Souta Sakabayashi, Takashi Morie, Makoto Nagata, and Atsushi Iwata
Email:{sake, morie, nagata, iwa}@dsl.hiroshima-u.ac.jp

Faculty of Engineering, Hiroshima University
Higashi-Hiroshima, 739-8527, JAPAN

ABSTRACT

This paper proposes a new arbitrary nonlinear transfer function generator circuit based on pulse-phase modulation. The circuit can generate an arbitrary non-monotone function with an identical circuit configuration. Chaotic signal generators using this function generator are also proposed. Circuit simulation results demonstrate that the new approach achieves high precision transformation. These circuits can be used for VLSI implementation of advanced neural networks such as associative memory models using non-monotone activation functions and chaotic neural networks.

KEYWORDS: non-monotone function, chaos, pulse-modulation, PWM, PPM

1. INTRODUCTION

Various nonlinear transfer functions, especially non-monotone functions, are used in advanced neural network models [1, 2]. Treating chaotic signals is also important for intelligent information processing [3, 4, 5]. If once a non-monotone function is made, chaotic signals are easily generated by feeding back the output to the input of the non-monotone function generator.

There have been several reports about non-monotone function / chaotic signal generation circuits using ordinary analog circuits in voltage or current domains. A voltage-mode chaos circuit [4] consists of op-amps, diodes and resistors. A current-mode chaos circuit [6] is designed using bipolar transistors as well as MOSFETs. The use of these circuit components is not suitable for ordinary VLSI using CMOS technology. From the standpoint of nonlinear transfer function generation, transfer function shapes generated by these analog circuits are strongly restricted by the characteristics of circuits or component devices. It is impossible to change function shapes arbitrarily. Accurate control of transfer functions is also difficult.

In our previous paper, arbitrary transfer function generators using a pulse-width modulation (PWM) method were proposed [7]. The PWM method is one approach toward achieving time-domain analog information processing using pulse signals. A new analog-digital merged circuit architecture using the PWM method has also been proposed [8]. In the architecture, weighted summation, which is an essential operation in neural networks, is easily performed using switched current sources. The PWM approach is suitable for large-scale integration of analog processing circuits because it matches the scaling trend in Si CMOS technology and leads to low voltage operation. The approach also achieves lower power consumption operation than traditional digital or pulse-density modulation (PDM) circuits because one data is represented by only one state transition in the PWM approach.

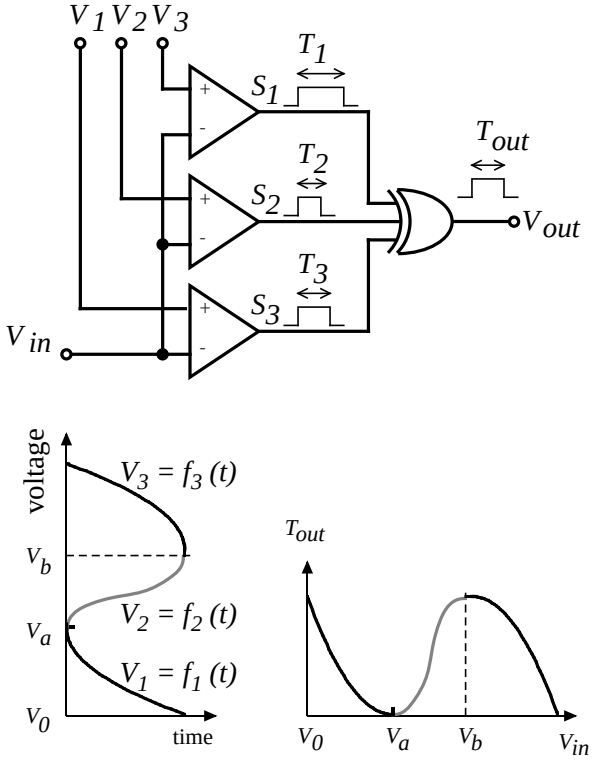


Figure 1: Third-order arbitrary transfer function generator circuit based on the previously proposed pulse-width modulation technique

A third-order arbitrary transfer function generator circuit based on the previously proposed technique [7] is shown in Fig. 1. PWM signals $S_i (i = 1, 2, 3)$ are made by comparing input voltage V_{in} with reference signals $V_i (i = 1, 2, 3)$. If the reference signal voltage V_i nonlinearly varies in the time domain, i.e. $V_i = f_i(t)$, where f_i is a nonlinear function, the pulse-width of signal S_i, T_i, expressed as a function of V_{in} is given by $T_i = f_i^{-1}(V_{in})$, where f_i^{-1} is the inverse function of f_i. Because function f_i is limited to a monotone function, we generate a non-monotone transfer function by combining the PWM signals $S_i (i = 1, 2, 3)$ using an exclusive-OR gate.

This circuit, however, has some drawbacks.

1. For generating non-monotone functions, plural comparators whose number is equal to that of monotone regions are required. This requirement increases the chip area and power consumption.

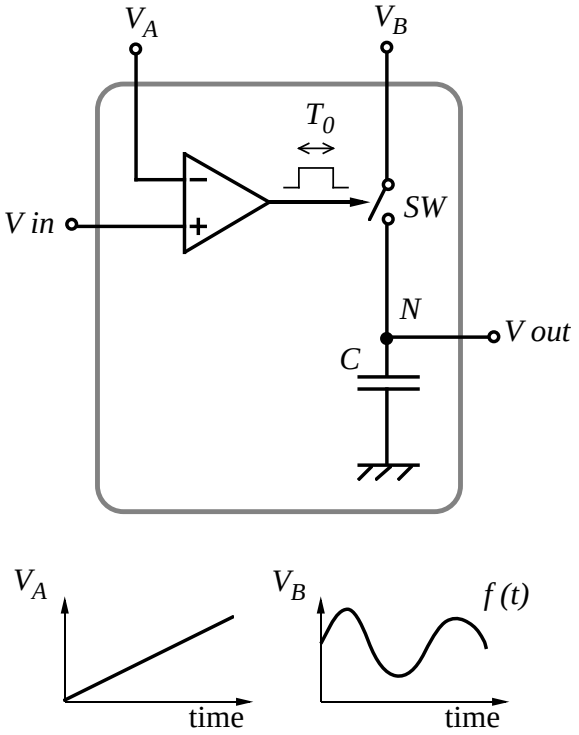


Figure 2: Arbitrary nonlinear non-monotone transfer function generator circuit

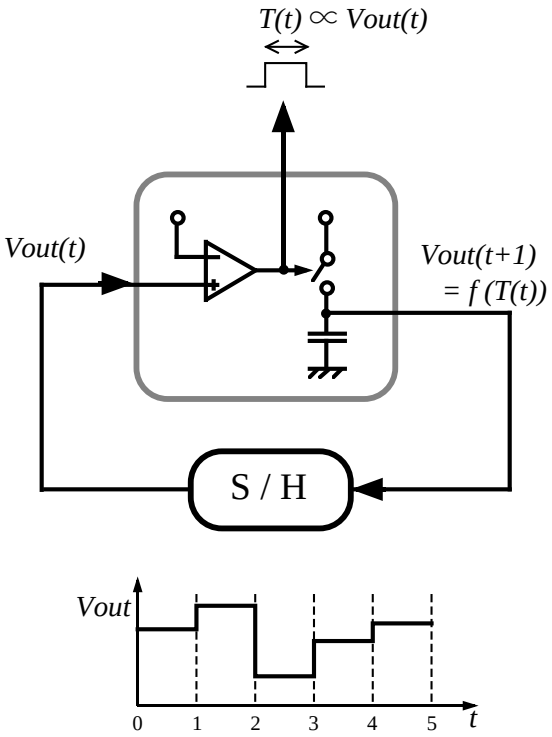


Figure 3: Chaotic signal generator

2. Plural reference signals whose waveforms correspond to the inverse function of the desired transfer function are required.

In this paper, we propose a new arbitrary nonlinear transfer function generator circuit based on pulse-phase modulation which overcomes the above drawbacks. The circuit can generate an arbitrary non-monotone function with an identical circuit configuration. Chaotic signal generators using this function generator circuit are also proposed, and their circuit simulation results demonstrate that the new approach achieves higher precision transformation than the previous one.

2. ARBITRARY FUNCTION GENERATORS BASED ON PULSE-PHASE MODULATION

The proposed circuit is shown in Fig. 2. This circuit generates an arbitrary non-monotone function with only one comparator. The basic operation of this circuit is as follows:

1. If the input is a voltage signal, input voltage V_{in} is linearly transformed into a pulse having width T_0. This transformation can be achieved by comparing V_{in} with a linearly ramped reference signal voltage V_A. If the input is a PWM signal, this transformation is obviously unnecessary.
2. A reference voltage V_B whose waveform shape is given by $f(t)$ is supplied to the capacitor node N through a switch SW, where we assume $V_B = f(0)$ at the leading edge of the PWM pulse. The switch SW is switched by the pulse signal, and is in the ON-state during period T_0. When the switch is turned off at the trailing edge of the pulse, the voltage of the capacitor node N, V_{out}, is kept at $f(T_0)$. Thus, we obtain $V_{out} = f(V_{in})$.

It is noted that $f(t)$ can be an arbitrary nonlinear non-monotone function as a function of time. Thus, this circuit is an arbitrary function generator. The realized transfer function is identical to the reference waveform shape, not the inverse function in the previously proposed approach. It is fairly easy to generate an arbitrary non-monotone waveform as a function of time by using various relaxation oscillator circuits or D/A converters, whereas it is very difficult to generate arbitrary nonlinear transfer functions using ordinary analog circuits in voltage or current domains. Furthermore, even when plural generator circuits operate simultaneously, only one reference waveform generator can be used, provided synchronous operation is assumed.

According to the operation principle, the timing when the switch SW is turned off is most important. The width of the pulse can be shortened provided the capacitor is charged up to voltage $f(T_0)$ during the pulse period. Thus, this approach for generating an arbitrary transfer function is based on *pulse-phase modulation (PPM)* or *pulse-timing modulation.*

The PPM approach is superior to the PWM approach from the viewpoint of power consumption because the latter approach consumes power for charging up and discharging capacitor C during pulse period T_0. However, to determine the signal value defined by a PPM pulse, the starting tim-

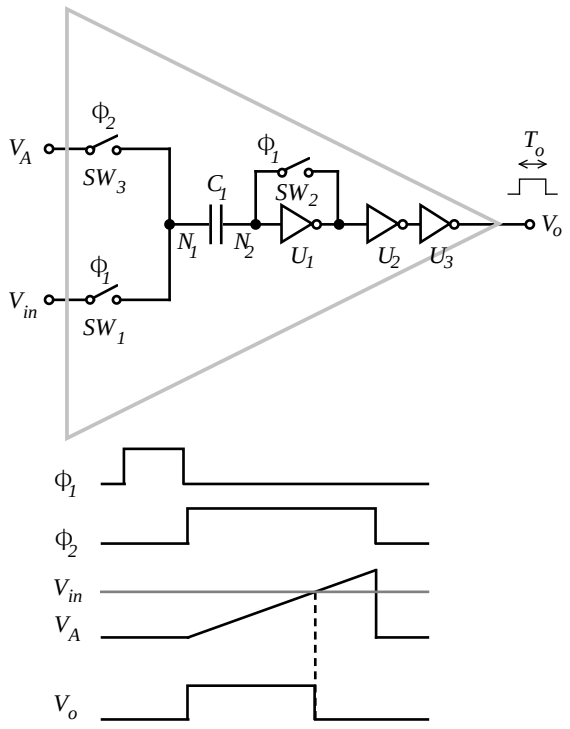


Figure 4: Comparator circuit including S/H mechanism

ing ($t = 0$) is needed. On the other hand, a PWM pulse includes the timing in itself. Thus, PWM signals are suitable for signal transmission.

As explained above, the proposed circuit outputs a voltage signal V_{out}. If we want a PWM pulse output, a voltage-to-pulse converter such as that in the first stage of the generator has to be added. If the output voltage signal is fed back to the input of the generator through a sample/hold (S/H) circuit as shown in Fig. 3, we can obtain the PWM pulse output generated in the previous time step. This circuit configuration corresponds just to the chaotic signal generator described in the next section.

A comparator circuit including an S/H mechanism is shown in Fig. 4. This comparator consists of inverters U_1 to U_3, a capacitor C_1, and switches SW_1 to SW_3 controlled by clocks ϕ_1 and ϕ_2. Capacitor C_1 holds the difference between the input voltage V_{in} and the threshold voltage of the inverter U_1, V_{th}, during the ϕ_1 period. In the ϕ_2 period, a ramped reference voltage V_A is supplied to the capacitor node N_1. When V_A reaches the V_{in}, the voltage of the other capacitor node (the input node of inverter U_1), N_2, reaches V_{th} and the inverter is inverted. Thus, an output pulse having a width T_0 is generated. In this comparator operation, the capacitor C_1 and the switch SW_1 operate as parts of the S/H circuit.

3. CIRCUIT SIMULATION RESULTS OF CHAOTIC SIGNAL GENERATORS

3.1. Chaos Generation Using Logistic Map

Chaotic behavior can be observed using a logistic map:

$$x(t+1) = 4ax(t)(1-x(t)), \quad (1)$$

where a is a parameter ranging from 0 to 1. The behavior of $x(t)$ is chaotic when $a > 0.89$.

This dynamics can be implemented by the chaotic signal generator with a reference waveform $f(t) = 4at(1-t)$. We performed a circuit simulation (HSPICE) of this circuit. The device parameters used were based on a 0.4 μm CMOS process, the supply voltage was 3.3 V, and the clock period was 800 nsec. Figure 5 shows the obtained return map. The relationship is almost perfectly parabolic. Figure 6 shows bifurcation diagrams obtained from HSPICE simulation of the previously proposed generator circuit (described in Sec. 1) (a) and the circuit proposed in this paper (b). The diagram for the former circuit is blurred; this is due to low calculation precision in the complex circuit. On the other hand, the diagram for the latter circuit has clear *windows* in the chaos region, and is nearly identical to the numerical simulation results. These results demonstrate that the circuit proposed in this paper is much superior in calculation precision.

3.2. Chaos Generation in A Chaotic Neuron Model

The dynamics of a chaotic neuron [9] is given by

$$\begin{aligned} y(t+1) &= ky(t) - \alpha u(y(t)) + a, \\ x(t+1) &= u(y(t+1)), \end{aligned} \quad (2)$$

where $y(t)$ and $x(t)$ are the internal state and the output of the neuron at the discrete time t, respectively; k, α and a are constants, and $u(y)$ is a logistic function.

$$u(y) = \frac{1}{1+\exp(-y/\varepsilon)}, \quad (3)$$

where ε is a constant. Figure 7 shows a return map of $y(t)$, where $k = 0.7$, $\alpha = 1$, $a = 0.5$, and $\varepsilon = 0.02$.

In order to implement this model by our circuits, we transformed variable y so that $y \geq 0$ because PWM signals are always positive; $y \to 2y - 1$.

A bifurcation diagram obtained from the HSPICE simulation is shown in Fig. 8. We obtained similar results to those in the numerical simulation [9].

4. CONCLUSION

We proposed a new arbitrary transfer function generator circuit based on pulse-phase modulation. This circuit can generate an arbitrary non-monotone function with an identical circuit configuration. The realized transfer function is identical to the reference waveform shape, which is easily generated by D/A conversion of digitally-stored waveform data.

Chaotic signal generators using this function generator circuit were also proposed. Circuit simulation (HSPICE) results of chaotic signal generators demonstrated that the new approach achieves much higher precision transformation than the previously proposed approach because of the much simpler circuit configuration.

References

[1] Morita, M., "Associative Memory with Nonmonotone Dynamics," *Neural Networks*, vol. 6, pp. 115–126, 1993.

[2] Kakeya, H. and Kindo, T., "Hierarchical Concept Formation in Associative Memory Composed of Neurowindow Elements," *Neural Networks*, vol. 9, no. 7, pp. 1095–1098, 1996.

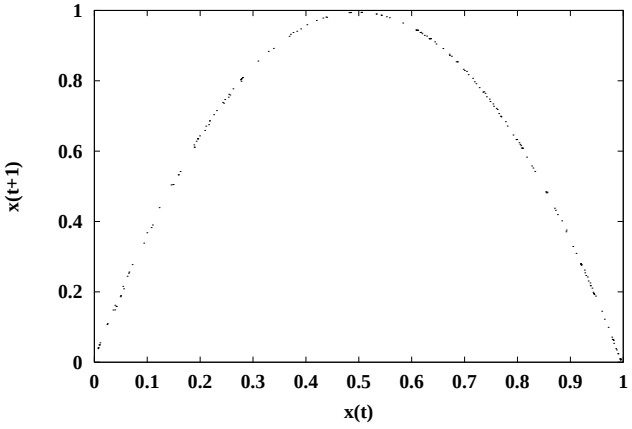
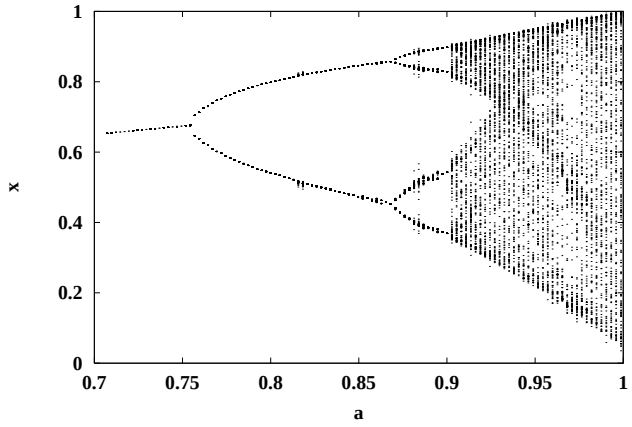
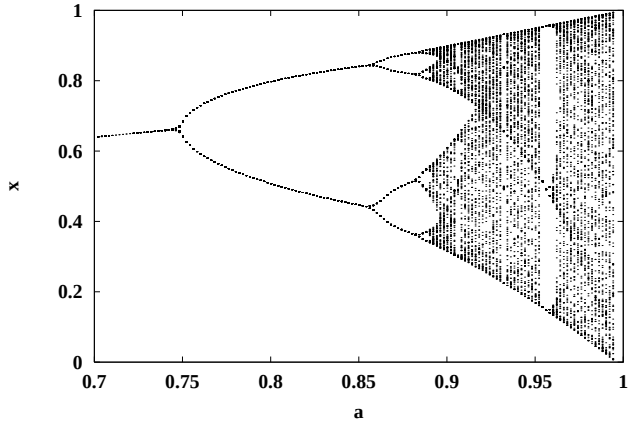


Figure 5: Return map of $x(t)$ in logistic map



(a) results using previously proposed circuits



(b) results using the new function generator

Figure 6: Bifurcation diagram of logistic map (HSPICE simulation)

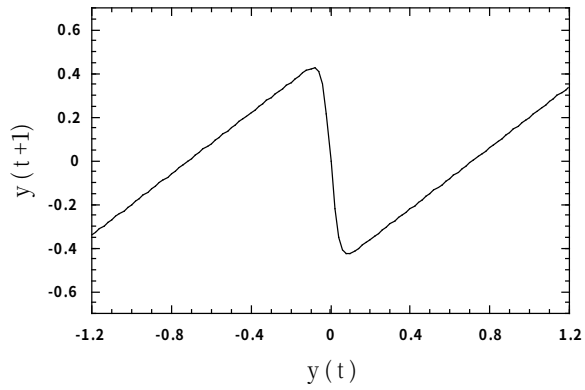


Figure 7: Return map of $y(t)$ in chaotic neuron model

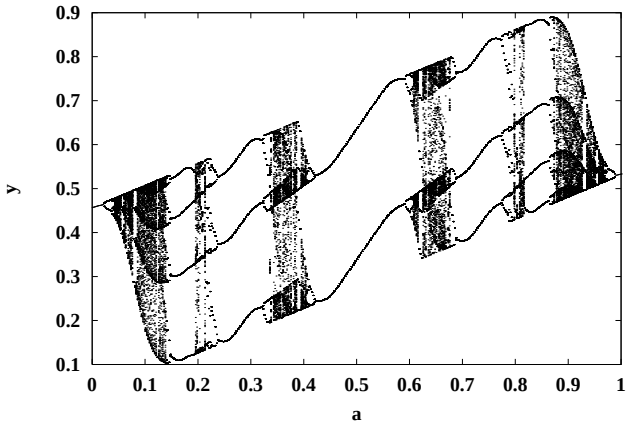


Figure 8: Bifurcation diagram in chaotic neuron model (HSPICE simulation)

[3] Nozawa, H., "A Neural Network Model as a Globally Coupled Map and Applications Based on Chaos," *Chaos*, vol. 2, no. 3, pp. 377–386, 1992.

[4] Miki, T., Shimono, M., and Yamakawa, T., "A Chaos Hardware Unit Employing the Peak Point Modulation," in *Proc. Int. Symp. Nonlinear Theory and its Applications*, pp. 25–30, 1995.

[5] Ishii, S., Fukumizo, K., and Watanabe, S., "A Network of Chaotic Elements for Information Processing," *Neural Networks*, vol. 9, pp. 25–40, 1996.

[6] Eguchi, K. and Inoue, T., "A Current-Mode Analog Chaos Circuit Realizing a Hénon Map," *IEICE Trans. Electron.*, vol. E80-C, no. 7, pp. 1063–1066, 1997.

[7] Morie, T., Sakabayashi, S., Nagata, M., and Iwata, A., "Nonlinear function generators and chaotic signal generators using a pulse-width modulation method," *Electron. Lett.*, vol. 33, no. 16, pp. 1351–1352, 1997.

[8] Iwata, A. and Nagata, M., "A Concept of Analog-Digital Merged Circuit Architecture for Future VLSI's," *IEICE Trans. Fundamentals.*, vol. E79-A, pp. 145–157, 1996.

[9] Aihara, K., Takabe, T., and Toyoda, M., "Chaotic Neural Networks," *Phys. Lett. A*, vol. 144, pp. 333–340, 1990.