A Multi-Functional Cellular Neural Network Circuit Using Pulse Modulation Signals for Image Recognition

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Abstract

This paper proposes a multi-functional cellular neural network (CNN) circuit based on arbitrary nonlinear function generation using pulse modulation signals. The proposed circuit implements discrete-time continuous-state CNN dynamics, and performs numerical calculations based on analog representations using pulse widths. We present a cell circuit that can implement a resistive-fuse network and a CNN-based Gabor-type filter, which are useful for image segmentation and feature extraction. We have designed a one-dimensional resistive-fuse network and a Gabor-type filter circuit using the cell circuit based on 0.6μm CMOS technology, and have verified their operation by using HSPICE simulation.

1 Introduction

Cellular neural networks or cellular nonlinear networks (CNN) provide an attractive paradigm for very large-scale integrated (VLSI) circuit architecture in applications devoted to pixel-parallel image processing.

The resistive-fuse network is well-known as an effective model for image segmentation, and some analog circuits implementing this model have been proposed [1].

Gabor filtering is an effective method for extracting the features of images, and it is known that such filtering is used in the human vision system. A flexible face recognition technique using this method has also been proposed [2]. To implement Gabor-type filtering using analog circuits, CNN models have been proposed, and analog circuits for them have been designed [3, 4].

Since the analog approach implements continuous-time and continuous-state dynamics, it achieves fast convergence. It also leads to the small circuit size, thus massively-parallel processing can be performed. However, a practical design for pixel-parallel analog CNN circuits corresponding to real image sizes (more than 100×100) is very difficult to realize because of unexpected parasitic components and various disturbance such as noise, interference, and device parameter mismatch. In addition, it is difficult for the analog approach to achieve arbitrary nonlinear transformation, thus various types of CNN models cannot be implemented by the same circuit.

A pulse-width modulation (PWM) approach is one technique for achieving time-domain analog information processing using pulse signals which have digital values in the voltage domain and analog values in the time domain. The PWM approach is suitable for the large-scale integration of analog processing circuits because it matches the scaling trend in Si CMOS technology and leads to low voltage operation. It also has high controllability and allows highly effective matching with ordinary digital systems. PWM circuits are stable and robust against various disturbances arising in real VLSI systems.

We have already proposed a circuit principle for arbitrary nonlinear transformation using conversion from a pulse-width/pulse-phase modulation (PWM/PPM) signal to analog voltage[5]. This principle makes it possible to realize arbitrary discrete-time continuous-state nonlinear dynamical systems. On the basis of this principle, we designed and fabricated an arbitrary chaos generator circuit, and tested its performance [6]. We also designed a nonlinear oscillator network circuit for image segmentation and verified its operation by using HSPICE simulation [7].

In this paper, we propose a CNN circuit with arbitrary nonlinear (non-monotone) functions based on pulse modulation techniques. In Sec. 2, we introduce pulse modulation circuit techniques for weighted summation and arbitrary nonlinear transformation, which are basic functions required for neural networks. In Sec. 3, we present a pulse modulation CNN circuit. In Sec. 4, as CNN models for image processing, resistive-fuse and Gabor-type filter networks are proposed, and their simulation results are presented. Finally, we provide the conclusion in Sec. 5.

2 Pulse Modulation Circuit Techniques for CNN

2.1 Weighted Summation

Inputs to a PWM circuit are PWM pulses. PWM input signals having pulse-width W_i, $(i = 1, 2, 3, \cdots)$, drive the corresponding current sources, and currents I_i flow to capacitor C_{in} during period W_i as shown in Fig. 1. The number of charges stored in the capacitor, Q_{sum}, and the terminal voltage of the capacitor, V_{sum}, are

$$Q_{sum} = \sum_i I_i W_i, \tag{1}$$

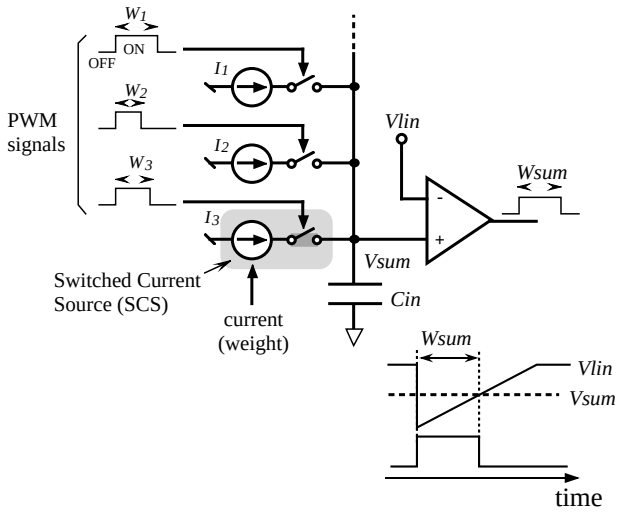


Figure 1: Weighted summation using PWM signals.

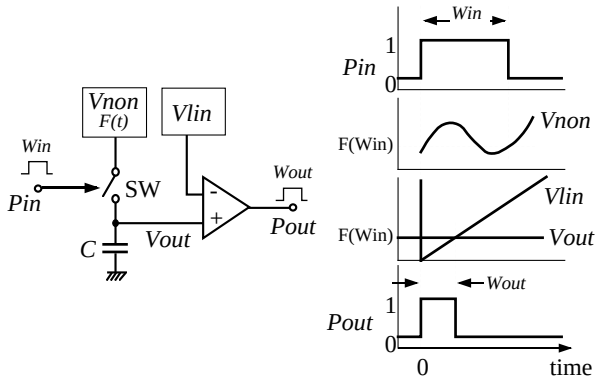


Figure 2: Principle of arbitrary nonlinear transformation using a PWM signal.

$$V_{sum} = \frac{Q_{sum}}{C_{in}} = \frac{\sum_i I_i W_i}{C_{in}},$$

respectively. Thus, the weighted summation result of the PWM data is obtained in the form of the number of stored charges or the terminal voltage of a capacitor. Then, voltage V_{sum} is linearly transformed into an output PWM pulse with a width of W_{sum} by comparing linearly-ramped reference voltage V_{lin}.

In CNN dynamics, positive and negative state-updating is required. Such bipolar updating can be achieved by charging or discharging the single capacitor by using positive and negative current sources.

2.2 Arbitrary Nonlinear Transformation

The principle of arbitrary nonlinear transformation using PWM signals is one of pulse-voltage conversion using a sample and hold operation of an arbitrary nonlinear voltage waveform $F(t)$ as shown in Fig. 2 [5].

The nonlinear transformation from PWM to PWM pulses proceeds as follows: Reference voltage V_{non} whose waveform in time-domain is given by an arbitrary nonlinear function $F(t)$ is supplied to capacitor C via switch SW. The switch is controlled by input PWM pulse P_{in}, where we assume $V_{non} = F(0)$ at the leading

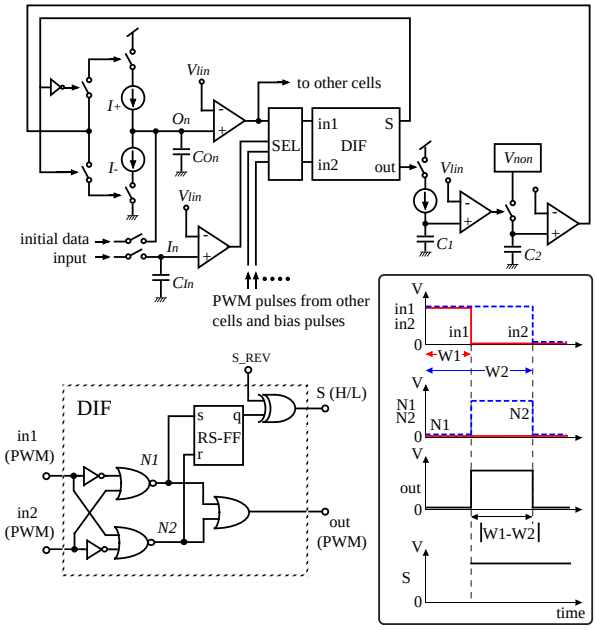


Figure 3: PWM CNN cell circuit.

edge of P_{in}. Switch SW is in the ON-state during period W_{in}. When the switch is turned off at the trailing edge of P_{in}, the voltage of the capacitor node, V_{out}, is kept at $F(W_{in})$. Thus, we obtain $V_{out} = F(V_{in})$. Voltage V_{out} is linearly transformed into output PWM pulse P_{out} by comparing linearly-ramped reference voltage V_{lin}. As a result, the relationship between the pulse widths of P_{in} and P_{out} is given by $W_{out} = F(W_{in})$.

Since the PWM-charges-PWM transformations are analog operations, much attention should be paid to the design of the corresponding circuits. However, establishing the design criteria in the present case is easier than in the pure analog approach because analog parts in PWM circuits are localized.

The reason this approach is useful is that it allows us to easily generate $F(t)$ by using various oscillator circuits or a combination of digital approaches (look-up tables or function generation) and D/A converters. In the latter case, basic waveform data are arbitrarily generated by digital circuits; in addition, the waveforms can be changed in realtime with high controllability. This means that the input-output functions can be changed arbitrarily and in realtime. Since a D/A converter operating at more than 100 MHz can be fabricated using sub-micron CMOS technology [8], the nonlinear transformation circuit can operate at more than 1 MHz with more than 6 bit precision. Because common waveform generators can be shared by many transformation circuits, the overhead of waveform generation is minimized.

3 A PWM CNN Circuit

A PWM circuit serially implements the discrete-time dynamics of CNN, although it spatially performs massively parallel operation. In contrast with pure analog circuit implementation, the PWM approach re-

quires more time to reach steady states, but it should have much higher controllability because it numerically solves the dynamics by using analog pulse widths.

A cell circuit of PWM CNN is shown in Fig. 3. The input and output of cell n are denoted by I_n and O_n, and are temporarily stored at capacitors C_{In} and C_{On}, respectively. The input value I_n and the initial value of O_n are downloaded from the host computer, and O_n is updated according to the following discrete-time dynamics.

$$O_n(t+1) - O_n(t) = \sum_{j,k \in N_n} G_{jk}(O_j - O_k) + F_j(O_j - I_n), \tag{2}$$

where N_n represents neighbor cells of n including cell n itself, and $G_{jk}(\cdot)$ and $F_j(\cdot)$ are arbitrary odd functions.

The updating process proceeds as follows:

1. Selector SEL selects a set of signals to be calculated, which corresponds to one term on the right side of Eq. 2.

2. The absolute value and the sign of the difference between the two signals such as $O_n - O_k$ or $O_n - I_n$ is calculated by circuit DIF. The absolute value and the sign bit are stored by capacitor C_1 and a flip-flop (RS-FF), respectively. The sign bit determines whether the positive or negative updating of O_n is performed.

3. The voltage stored in capacitor C_1 is converted into a PWM pulse, and it switches the voltage source V_{non} whose voltage waveform in the time domain is the same as the corresponding (nonlinear) function ($G_{jk}(\cdot)$ or $F_j(\cdot)$). Thus, capacitor C_2 holds the value of the corresponding term in Eq. 2.

4. The voltage stored in capacitor C_2 is again converted into a PWM pulse, and it switches the current source I_+ or I_-. Output O_n is thus updated by the corresponding term.

5. Repeating the above processes, O_n is updated by another term.

4 CNN models for image processing

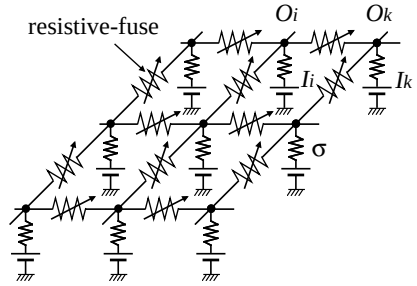
4.1 Resistive-Fuse Network Model

The resistive-fuse network is shown in Fig. 4. The steady state of the network is obtained by minimizing the following function E [1]:

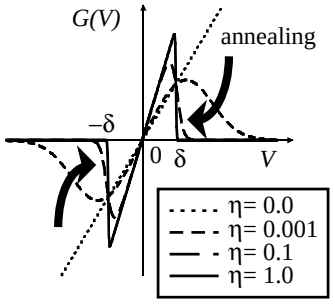
$$E = \sum_n \sum_{k \in N_n} \int_0^{O_n - O_k} G(V)dV + \frac{\sigma}{2} \sum_n (O_n - I_n)^2, \tag{3}$$

where, σ is a constant, and $G(\cdot)$ is the current-voltage characteristic of the resistive-fuse shown in Fig. 4(b). It is given by

$$G(V) = \left[\frac{1}{1 + \exp(-2\eta(\delta^2 - V^2))} \right] \frac{V}{R}, \tag{4}$$



(a) resistive-fuse network



(b) resistive-fuse characteristic

Figure 4: Resistive-fuse network model.

where, η, δ and R are constants. This resistive-fuse device is considered a linear resistor when $\eta = 0$, while it is a complete resistive-fuse when $\eta = 1$; the neighboring cells are disconnected when $O_n - O_k > \delta$, and edge detection is performed, while the resistance is linear when $O_n - O_k \leq \delta$, and a smoothing process is performed.

The PWM CNN circuit obtains the minimum of E by using a steepest descent method:

$$O_n(t+1) = O_n(t) - \nu \frac{\partial E}{\partial O_n}, \tag{5}$$

$$\frac{\partial E}{\partial O_n} = \sum_n \sum_{k \in N_n} G(O_n - O_k) + \sigma \sum_n (O_n - I_n), \tag{6}$$

where ν is a constant. To avoid reaching local minima, the circuit performs an annealing process by changing the shape of $G(\cdot)$, i.e., by increasing parameter η, as shown in Fig. 4(b).

We have designed a 1-D resistive-fuse network circuit with 20 cells. The result of HSPICE simulation is shown in Fig. 5. It verifies that the PWM CNN circuit operates as a resistive-fuse network, and it simultaneously performs edge detection and smoothing, thus image segmentation is achieved.

4.2 CNN-based Gabor-type Filtering

A 1-D CNN circuit performing Gabor-type filtering is shown in Fig. 6 [3]. The cell consists of two nodes corresponding to real and imaginary parts. The convolution kernel realized in this circuit is

$$h(n) = \frac{\lambda}{2} e^{-\lambda|n|} e^{j\omega_0 n}, \tag{7}$$

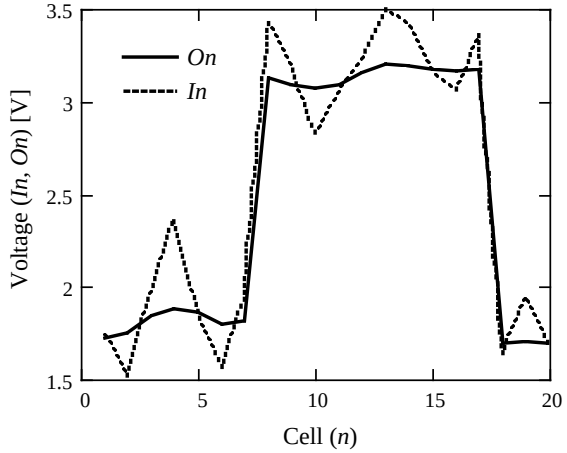


Figure 5: HSPICE simulation result of a resistive-fuse network using the PWM CNN circuit.

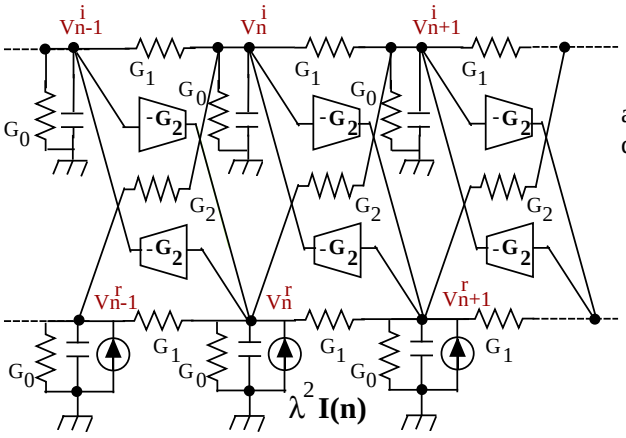


Figure 6: 1-D CNN circuit performing Gabor-type filtering, where $G_0 = 2+\lambda^2-2\cos\omega_0-\sin\omega_0$, $G_1 = \cos\omega_0$, $G_2 = \sin\omega_0$.

where λ is a constant, and ω_0 is a frequency.

The dynamics of this circuit are expressed by two node voltages v^r and v^i for each cell:

$$\begin{aligned}\begin{bmatrix} \dot{v}_n^r \\ \dot{v}_n^i \end{bmatrix} &= \begin{bmatrix} \cos\omega_0 & -\sin\omega_0 \\ \sin\omega_0 & \cos\omega_0 \end{bmatrix} \begin{bmatrix} v_{n-1}^r \\ v_{n-1}^i \end{bmatrix} \\ &- \begin{bmatrix} 2+\lambda^2 & 0 \\ 0 & 2+\lambda^2 \end{bmatrix} \begin{bmatrix} v_n^r \\ v_n^i \end{bmatrix} \\ &+ \begin{bmatrix} \cos\omega_0 & \sin\omega_0 \\ -\sin\omega_0 & \cos\omega_0 \end{bmatrix} \begin{bmatrix} v_{n+1}^r \\ v_{n+1}^i \end{bmatrix} \\ &+ \begin{bmatrix} \lambda^2 I_n \\ 0 \end{bmatrix}. \end{aligned} \tag{8}$$

In order to implement these dynamics in our PWM CNN circuit, this equation is modified so that each term is expressed by a difference between two variables (or between a variable and a constant). Since variables v^r and v^i can be positive or negative, we define W_0 as the pulse width corresponding to zero value, and represent negative value by a PWM pulse with a width less than W_0.

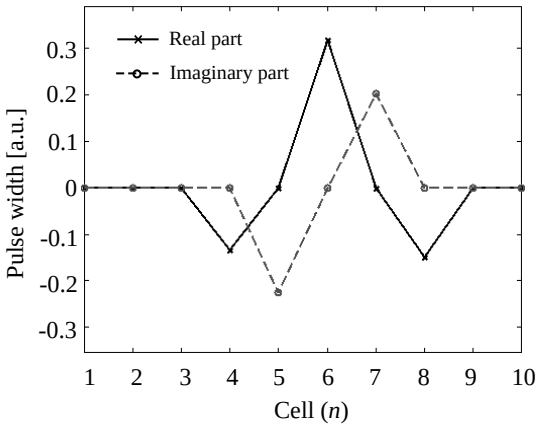


Figure 7: HSPICE simulation result of a 1-D Gabor-type filter using the PWM CNN circuit. The input is only given at the sixth cell. $\lambda = 0.7, \omega_0 = \pi/4$.

By using widths of PWM signals, W, instead of voltages v in Eq. 8, we obtain the following discrete-time dynamics for our PWM CNN circuit:

$$\begin{aligned} \Delta W^r &\equiv W^r(t+1) - W^r(t) \\ &= \lambda^2(I_n - W_0) \\ &+ \cos\omega_0 \cdot (W_{n-1}^r - W_0) \\ &+ \cos\omega_0 \cdot (W_{n+1}^r - W_0) \\ &+ \sin\omega_0 \cdot (W_{n+1}^i - W_{n-1}^i) \\ &- (2+\lambda^2)(W_n^r - W_0), \\ \Delta W^i &\equiv W^i(t+1) - W^i(t) \\ &= \cos\omega_0 \cdot (W_{n-1}^i - W_0) \\ &+ \cos\omega_0 \cdot (W_{n+1}^i - W_0) \\ &- \sin\omega_0 \cdot (W_{n+1}^r - W_{n-1}^r) \\ &- (2+\lambda^2)(W_n^i - W_0). \end{aligned} \tag{9}$$

We have designed a 1-D Gabor-type filter circuit with 10 cells, each of which consists of two PWM CNN cell circuits. The result of HSPICE simulation is shown in Fig. 7. It verifies that the PWM CNN circuit operates as a Gabor-type filter circuit.

5 Conclusion

We proposed a multi-functional CNN circuit based on arbitrary nonlinear function generation using PWM signals. This PWM circuit serially implements the discrete-time dynamics of the CNN while it spatially performs massively-parallel operation. Although the PWM approach requires more time to reach steady states than does the pure analog approach, it should provide much greater controllability and robustness because it numerically solves the dynamics by using analog pulse widths. By using the basic cell circuit, we designed a 1-D resistive-fuse network and a Gabor-type filter circuit based on 0.6μm CMOS technology, and verified their operation by using HSPICE simulation.

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References

[1] J. Harris, C. Koch, and J. Luo, "Resistive Fuses: Analog Hardware for Detecting Discontinuities in Early Vision," in C. Mead and M. Ismail, editors, *Analog VLSI Implementation of Neural Systems*, pp. 27–55. Kluwer Academic Publishers, 1989.

[2] M. Lades, J. C. Vorbrüggen, J. Buhmann, J. Lange, C. v.d. Malsburg, R. P. Würtz, and W. Konen, "Distortion Invariant Object Recognition in the Dynamic Link Architecture," *IEEE Trans. Comput.*, vol. 42, no. 3, pp. 300–311, 1993.

[3] B. E. Shi, "Gabor-Type Filtering in Space and Time with Cellular Neural Networks," *IEEE Trans. Circuits & Syst. I*, vol. 45, pp. 121–132, 1998.

[4] B. E. Shi, "2D Focal Plane Steerable and Scalable Cortial Filters," in *Proc. Int. Conf. on Microelectronics for Neural, Fuzzy and Bio-inspired Systems (MicroNeuro)*, pp. 232–239, 1999.

[5] T. Morie, S. Sakabayashi, H. Ando, M. Nagata, and A. Iwata, "Pulse Modulation Circuit Techniques for Nonlinear Dynamical Systems," in *Proc. Int. Symp. on Nonlinear Theory and its Application (NOLTA'98)*, pp. 447–450, Crans-Montana, Sept. 1998.

[6] K. Murakoshi, T. Morie, M. Nagata, and A. Iwata, "An Arbitrary Chaos Generator Core Circuit Using PWM/PPM Signals," in *Asia and South Pacific Design Automation Conference (ASD-DAC2000)*, pp. 100–101, Tokyo, Jan. 2000.

[7] H. Ando, M. Miyake, T. Morie, M. Nagata, and A. Iwata, "A Nonlinear Oscillator Network for Gray-level Image Segmentation and PWM/PPM Circuits for Its VLSI Implementation," *IEICE Trans. Fundamentals.*, vol. E83-A, no. 2, pp. 329–336, 2000.

[8] J. M. Fournier and P. Senn, "A 130-MHz 8-b CMOS Video DAC for HDTV Applications," *IEEE J. Solid-State Circuits*, vol. 26, no. 7, pp. 1073–1077, 1991.