An Arbitrary Chaos Generator Core Circuit Using PWM/PPM Signals

Kenichi Murakoshi, Takashi Morie, Makoto Nagata, and Atsushi Iwata
Faculty of Engineering, Hiroshima University
Higashi-Hiroshima, 739-8527 Japan
{ken,morie,nagata,iwa}@dsl.hiroshima-u.ac.jp

Abstract— A compact chaos generator core circuit has been designed, fabricated, and tested. It generates PWM and PPM (pulse width and phase modulation) signals that follow arbitrary nonlinear analog dynamics. The measurement results show that PWM/PPM chaotic signals are generated at 1 MHz with a calculation precision of 6.7 bits at a supply voltage of 3.3 V. The circuit can be used for large-scale integrated noise sources or high-performance advanced neural networks using nonlinear analog dynamics.

I. Introduction

Many recent studies in neural information processing have revealed the important role of nonlinear analog dynamics. Chaotic neural networks are a typical example. The implementation of various theoretical models utilizing chaos on a chip requires a compact arbitrary chaos generator circuit. However, conventional VLSI circuits cannot sufficiently implement such nonlinear dynamics. Essentially, digital approaches cannot implement analog dynamics, although they offer high precision and controllability. A digital approach requires a large circuit area, and massively parallel operation on a chip is difficult. Analog approaches are immediately more suitable for realizing analog dynamical systems, though they make it difficult to achieve arbitrary nonlinear and non-monotone transformation; the transformation functions achieved by the analog approach strongly depend on the characteristics of devices and/or circuits used.

We present here a new arbitrary chaos generator core circuit using PWM/PPM (pulse-width modulation/pulse-phase modulation) signals.

II. Architecture and core circuit

The basic principle of the circuit operation is one of PWM-voltage conversion using a sample and hold operation of an arbitrary nonlinear voltage waveform [1]. The chaos generator core circuit is shown in Fig. 1. It consists of a clocked CMOS comparator including CMOS inverters, a capacitor and switches; a PWM-PPM converter using a delay in the form of an inverter chain; and a simple control circuit. This core circuit does not include analog components, thus it can be shrunk with a scaling trend in CMOS fabrication technology. It has the advantage of low power consumption, and is suitable for low-voltage operation.

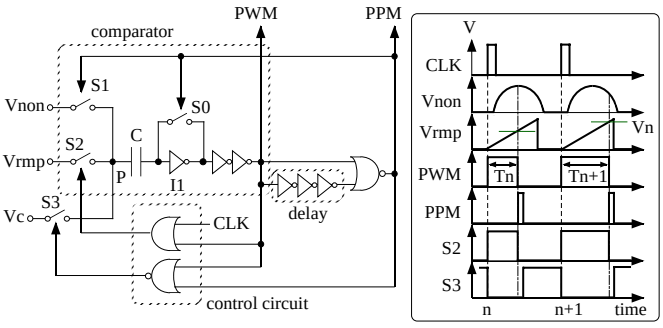

Fig. 1. Arbitrary chaos generator core circuit and timing diagram.

The circuit operation proceeds as follows. Here, the time step n is defined by the clock signal CLK and V_n indicates a voltage at each time step. It is assumed that capacitor C holds the voltage difference between an initial voltage V_0 and the threshold voltage of inverter $I1$. At the initial time step (n=0), switch $S2$ is turned on by CLK, and the ramped voltage V_{rmp} is supplied at node P. When the voltage of node P reaches V_0, $I1$ inverts and PWM and PPM signals are generated. The PPM signal turns on $S0$ and $S1$, and capacitor C holds the voltage of V_{non} at that timing; this creates V_1. After $S1$ turns off, $S3$ turns on and node P is fixed at a constant voltage V_c. The same operation is repeated at the next time step (n=1). Thus, if the waveform V_{non} varies as $V_{non}(t) = f(t)$ and V_{rmp} is linearly ramped, then the pulse width of PWM signals or the pulse timing of PPM signals T_n is updated as follows: $T_{n+1} = f(T_n)$.

Nonlinear voltage waveform $V_{non}(t)$ can be generated by digital circuits and D/A converters. Waveform generation by the digital approach allows high flexibility and high controllability. If the waveform is smoothed by an additional low-pass filter, chaos generation can be achieved even if the digital circuit has fairly low bit precision. Although this waveform generator causes overhead, a common generator can be shared by multiple chaos generator circuits in many applications, such as that of artificial neural networks.

The circuit was designed and fabricated using a 0.6 μm CMOS 2-poly 3-metal technology. The photograph of the circuit is shown in Fig. 2. The circuit area is 100 $\times$ 100 μm sq.

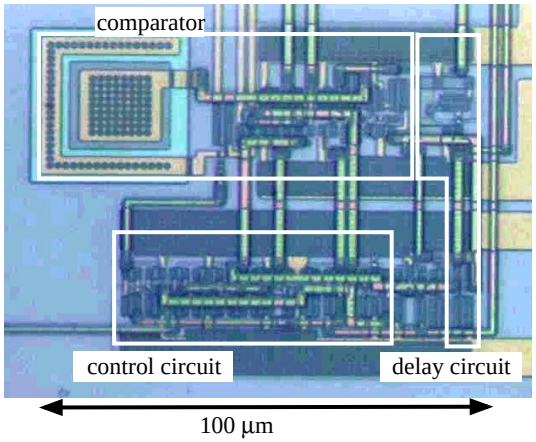

Fig. 2. Micro-photograph of the chaos generator circuit.

The capacitance of C, which was set at 1 pF in order to reduce the effect of clock-feedthrough, can be reduced by optimizing the circuit design in accordance with the required calculation precision. The power dissipation was estimated to be 200 μW at $V_{DD} = 3.3$ V from SPICE simulation.

III. Measurement results

We measured the fabricated circuit. The power supply voltage was 3.3 V, and the clock period was 1 μs. The maximum width of the PWM pulses and the width of PPM pulses were set at 760 ns and 10 ns, respectively. The waveforms V_{rmp} and V_{non} were supplied by an arbitrary waveform generator (Tektronix: AWG2021, 250MHz). The operating speed is determined by the required resolution. In this measurement, the time resolution of V_{non} was more than 7 bits. It is noted that chaotic operation is achieved because the waveform of V_{non} is not strictly quantized.

As a simple example of chaos, we generated an iterated logistic map: $x_{n+1} = 4ax_n(1-x_n)$, where a is a bifurcation parameter ranging from 0 to 1. In order to realize this dynamics, we used a waveform of $V_{non}(t) = 4at(1-t)$.

The reference waveforms (CLK, V_{rmp}, and V_{non}) and the PWM and PPM outputs are shown in Figs. 3. We observed chaotic behavior in the time series of the PWM and PPM outputs. A return map obtained from the PWM outputs is shown in Figs. 4. We obtained a calculation precision of 6.7 bits.

IV. Conclusion

The core circuit described here is useful for large-scale integrated noise sources, the noise characteristics of which can be changed arbitrarily and in realtime. The circuit is also useful for high-performance advanced neural networks using nonlinear analog dynamics.

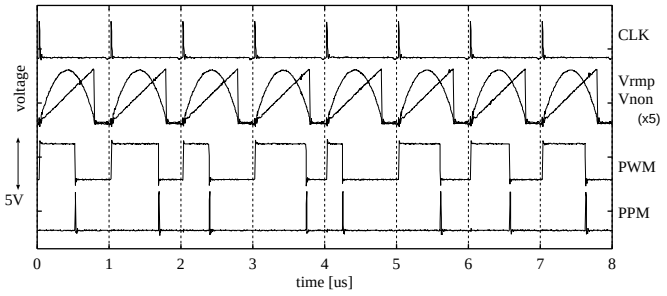

Fig. 3. Reference waveforms and PWM/PPM outputs for iterated logistic map. Each waveform is shifted arbitrarily along the vertical axis, and the starting time is arbitrary.

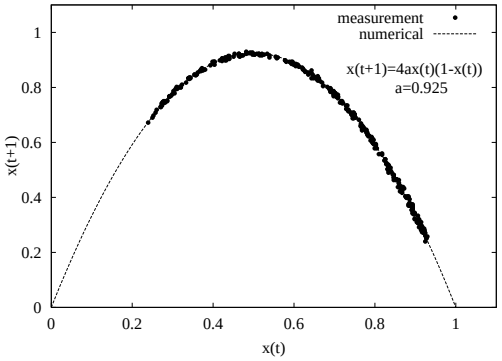

Fig. 4. Return map generated by the chaos generator circuit.

Acknowledgments

This work was supported by the Ministry of Education, Science, Sports, and Culture under Grant-in-Aid for Scientific Research on Priority Areas (Number: 269). This work was supported in part by The Mazda Foundation's Research Grant. The VLSI chip was fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

References

[1] T. Morie, S. Sakabayashi, H. Ando, M. Nagata, and A. Iwata, "Pulse modulation circuit techniques for nonlinear dynamical systems," in *Proc. Int. Symp. on Nonlinear Theory and its Applications (NOLTA'98)*, pp. 447–450, Crans-Montana, Sept. 1998.